

W.T.S

**DEVELOPMENT OF PASSIVATION TECHNOLOGY FOR
IMPROVED GaN/AlGa_N HEMT PERFORMANCE AND
RELIABILITY**

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Performance Report
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13. ABSTRACT (Maximum 200 words) Under the support of this contract, we have been successful in mitigating the current collapse that is found in nitride based high electron mobility transistors (HEMTs) that is responsible for low power performance from these devices. We have successfully and repeatedly grown oxide material that, along with surface cleaning recipes, reduce the surface states and reduce the device-device surface leakage. As part of the recipe development we have studied fundamental characteristics of the native oxides on GaN and AlGaIn surfaces using XPS and compared the results to oxides generated by exposure to UV ozone. We have developed a lattice matched oxide, magnesium calcium oxide (MgCaO), and deposition recipe that provides for the lowest level of surface traps and thus the highest level of surface passivation. Along with this oxide, we have shown that a thin layer of scandium oxide (Sc2O3), approximately 5nm thick, is sufficient for protection of environmental degradation of the MgCaO in environments of 100% humidity and elevated temperatures. This oxide/nitride interface is also able to withstand the processing temperatures of the nitride based HEMTs.					
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2.0 Objectives

2.1 Task 1: Structure Development

Clearly the composition of the cap layer plays a significant role in the effectiveness of the passivation. This is most likely related to the relative removal rate of the oxides formed on GaN surfaces versus the removal rate from surfaces containing Al. We have begun an initial investigation into the nature of the oxide formed on GaN during the ozone pre-cleaning treatment needed for the MBE-based deposition process. Under this program we will expand this study to include surfaces with varying amounts of Al. The composition of the surface oxides will be investigated using depth profiling XPS. This information will be correlated with the removal behavior of each oxide as determined in the MBE chamber using RHEED. In particular the temperature needed to desorb each oxide will be determined. It is likely that higher aluminum concentrations may produce oxides with increased thermal stability, making it difficult to completely remove the contamination layer without degrading the gate metal. On the other hand, higher aluminum concentrations may produce a more stable interface with the dielectric. The optimum cap layer will be determined by examining the degree of passivation and the gate leakage before and after passivation using the cleaning recipes developed from the XPS and RHEED data for each cap composition. The various heterostructures and devices needed for this study will be supplied by WPAFB. The passivation and characterization will be performed at UF.

2.2 Task 2: Improved Contact Metallization

For all of the dielectrics we have studied thus far we have observed an increase in the gate leakage current which we attribute to degradation of the gate metal during the elevated temperature needed for cleaning prior to dielectric deposition. We propose to study this degradation and develop gate metals with improved thermal stability. For the Ohmics we plan to investigate refractory metals such as W or W-based silicides, WSix. In order to achieve good Ohmic contact behavior it may be necessary to make a composite contact with W on the top and thin layers of TiAl between the GaN and the W. For gate metallization we will investigate Pt/Au. All of these metallization schemes will be tested for thermal and electrical stability and reliability. Auger electron spectroscopy (AES) will be used to investigate the amount and type of interfacial layers formed as a function of annealing temperature.

2.3 Task 3: Optimized Dielectric Deposition

From initial studies, it appears that cleaning of the top nitride surface is critical to attaining the optimum passivation. Normally such cleaning would be performed by heating the wafer to temperatures near the desorption temperature for Ga_2O_3 which is $\sim 600^\circ\text{C}$. Such temperatures cannot be used for HEMT passivation due to the thermal instability of the gate metal. In order to improve the cleaning at the necessary low temperatures, $<400^\circ\text{C}$, we will investigate the effectiveness of in-situ hydrogen plasma cleaning using an RF plasma source. In addition to measuring the effect of the hydrogen on the surface composition and subsequent passivation, we will also investigate the effect of plasma exposure to the gate and ohmic metals. If degradation is observed, then metals

with superior resistance to plasma damage will be investigated as part of Task 2. The effect of hydrogen plasma cleaning on caps with various compositions will also be studied in concert with Task 1.

Another area in which improved performance may be achieved is in the dielectric microstructure and composition. It is known for MgO and suspected for Sc_2O_3 that the first few atomic layers deposited on the GaN are epitaxial. After roughly 2-4 nm the growth front breaks down and the material becomes textured nanocrystalline. It is this combination of microstructures which allows the low D_{it} , low- $10^{11} \text{ eV}^{-1}\text{cm}^{-2}$ for MgO for example, and high breakdown, 3-4 MV/cm. It is believed that by improving the quality of the epitaxial portion of the layer, the passivation and ultimately perhaps even the reliability, could be improved as well. One way to improve the interfacial layer quality is to reduce the 6.6% lattice mismatch between the MgO and the GaN. CaO has similar electrical properties to MgO but has an atomic spacing which is larger than that of GaN. Since CaO and MgO are completely miscible, it should be possible to make a lattice matched interfacial layer. It is likely that this layer will exhibit superior electrical and thermal properties over the more mismatched MgO/GaN interface.

As discussed in Task 4, environmental stability is also an issue with the MgO dielectric. It is believed that capping of the MgO may be sufficient to suppress this degradation. Preliminary studies suggest that Sc_2O_3 is more robust than the MgO and as such may prove to be an ideal capping material. Should a composite dielectric cap be required in order to achieve the desired stability, deposition of graded passivation layers which begin with MgO or CaMgO and end with Sc_2O_3 will be explored.

2.4 Task 4: Electrical and Environmental Stability

As discussed in the background section we have observed degradation of the MgO after long term exposure to air. This degradation is believed to be due to interaction with water vapor in the air to form MgOH species. We have found that capping of the MgO, for example with the gate metal in a MOS diode, effectively suppresses this degradation. Thus one approach to achieving long term environmental stability may simply involve capping of the passivation layer with SiNx. The effectiveness of this approach will be tested by monitoring the power performance of MgO passivated HEMTs over a period of months. Companion devices using Sc_2O_3 which do not show this degradation will also be tested for comparison. Should SiNx not prove feasible then capping of the MgO with Sc_2O_3 as described in Task 3 will also be explored.

In addition to environmental stability, it is also necessary for the passivated devices to possess good electrical stability. We will also test this aspect of device reliability by stressing passivated devices at a constant current for long periods of time and periodically monitoring their DC and RF performance. The resistance to degradation will be correlated with the information gathered about the microstructure and composition in order to determine the optimum interfacial structure.

3.0 Status of Effort (200 words)

Under the support of this contract, we have been successful in mitigating the current collapse that is found in nitride based high electron mobility transistors (HEMTs) that is responsible for low power performance from these devices. We have been able to upgrade our oxide deposition system for 3" wafer uniformity and have successfully and repeatedly grown oxide material that, along with surface cleaning recipes, reduce the surface states and reduce the device-device surface leakage. As part of the recipe development we have studied fundamental characteristics of the native oxides on GaN and AlGaN surfaces using XPS and compared the results to oxides generated by exposure to UV ozone. We have developed a lattice matched oxide, magnesium calcium oxide (MgCaO), and deposition recipe that provides for the lowest level of surface traps and thus the highest level of surface passivation. Along with this oxide, we have shown that a thin layer of scandium oxide (Sc_2O_3), approximately 5nm thick, is sufficient for protection of environmental degradation of the MgCaO in environments of 100% humidity and elevated temperatures. This oxide/nitride interface is also able to withstand the processing temperatures of the nitride based HEMTs.

4.0 Accomplishments/New Findings

4.1 Task 1: Structure Development

- 4.1.1 XPS studies of oxide/GaN and oxide/AlGaN surfaces formed with and without UV ozone exposure
- 4.1.2 Effect of UV Ozone exposure on SiNx passivation of AlGaN capped HEMTs
- 4.1.3 Effect of Free Standing GaN Substrates on DC Characteristics of AlGaN/GaN Heterostructure Field-Effect Transistors
- 4.1.4 X-TEM of AlGaN/GaN HEMT devices
- 4.1.5 Low temperature GaN growth for AlGaN post-process capping
- 4.1.6 UV-ozone as a screening method for HEMT devices
- 4.1.7 UV-ozone effects on surface oxynitride composition

4.2 Task 2: Improved Contact Metallization

- 4.2.1 Thermal stability of Ir gates and final metal
- 4.2.2 Passivation treatment effects on source and drain contact resistance

4.3 Task 3: Optimized Dielectric Deposition

- 4.3.1 Upgrade of oxide GSMBE system to 2" or 3" wafer capability
- 4.3.2 Determination and optimization of dielectric microstructure
- 4.3.3 Device Improvement through the use of Sc₂O₃ For Both Passivation and Gate Dielectric
- 4.3.4 Growth of CaO
- 4.3.5 Growth of Ternary MgCaO
- 4.3.6 UV effects on isolation current
- 4.3.7 Effects of MgCaO composition on passivation and Sc₂O₃ capping
- 4.3.8 Other applications of oxide and surface treatment recipes

4.4 Task 4: Electrical and Environmental Stability

- 4.4.1 Scandium Oxide capping of crystalline dielectrics
- 4.4.2 Stability of the crystalline oxides in accelerated aging experiments
- 4.4.3 Passivation of Hall effect samples and aging
- 4.4.4 Passivation of HEMT devices and aging of dielectric films at elevated temperatures

4.1 Task 1: Structure Development

4.1.1 XPS studies of oxide/GaN and oxide/AlGaN surfaces formed with and without UV ozone exposure

We have observed a clear dependence of the effectiveness of the passivation on the composition of the cap design. This is most likely related to the relative removal rate of the oxides formed on GaN surfaces versus the removal rate from surfaces containing Al. We have begun an initial investigation into the nature of the native oxides on GaN and AlGaN surfaces as well as those formed during the ozone pre-cleaning treatment needed for the MBE-based deposition process. The surface of GaN and AlGaN terminated HEMT structures was studied using XPS to determine the nature of the surface oxide and surface charge effects. As received GaN and AlGaN surfaces were examined in XPS. These surfaces showed a thin (few monolayers) native oxide which held approximately 1 eV surface charge, shown in Figures 4.1.1 and 4.1.2.

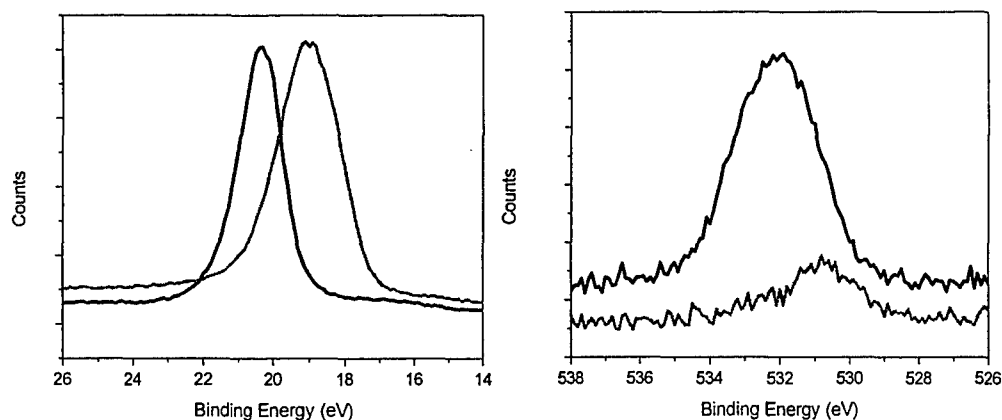


Figure 4.1.1. XPS spectra of Ga 3d (at left) and O 1s (at right) taken from as received GaN capped HEMT without exposure to UV ozone. The blue curve was taken before sputtering while the green curve was taken after a 2 min. Ar sputter.

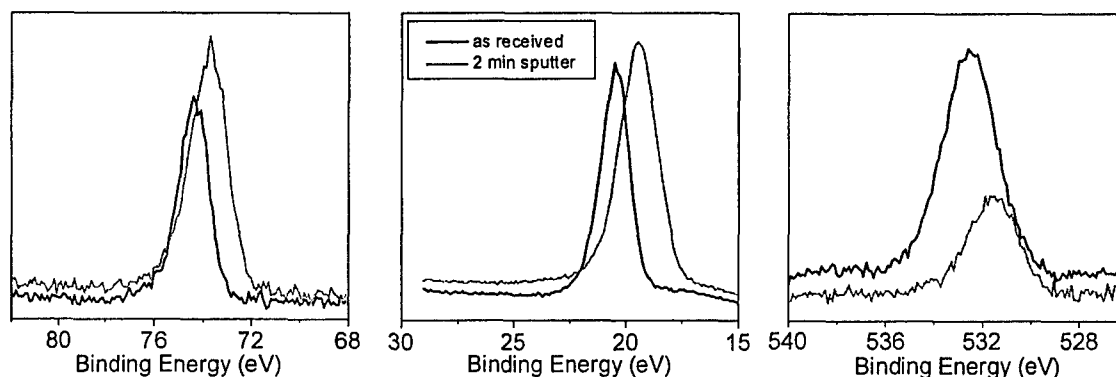


Figure 4.1.2. Spectra taken from as received AlGaN capped HEMT without exposure to UV ozone: Al 2p (left), Ga 3d (center), and O 1s (right). Blue is as received, green is after 2 min. Ar sputter.

Our current recipe for passivation includes a 25 minute exposure to UV-ozone. Thus the samples were then exposed to UV-ozone for 25 minutes at room temperature in the UVOCS ozone system. The GaN surface oxide showed a mix of GaOx and GaN and held a surface charge of 5eV, shown in Figure 4.1.3. The surface charge was measured by determining the shift in the entire XPS spectrum. The charge was reduced as the surface oxide was sputtered away and appeared to be dependant upon the surface oxide thickness, which was determined by the intensity of the O 1s peak. The AlGaIn surface oxide, shown in Figure 4.1.4, showed a mix of AlOx, GaOx, GaN, AlN and held a surface charge of 1eV, 4eV less than the GaN surface oxide. This charge was reduced as the surface oxide was sputtered away as well. Both surface oxides appeared to be similar in thickness, however, the GaN surface oxide appears to be more insulating, given its greater ability to hold a surface charge.

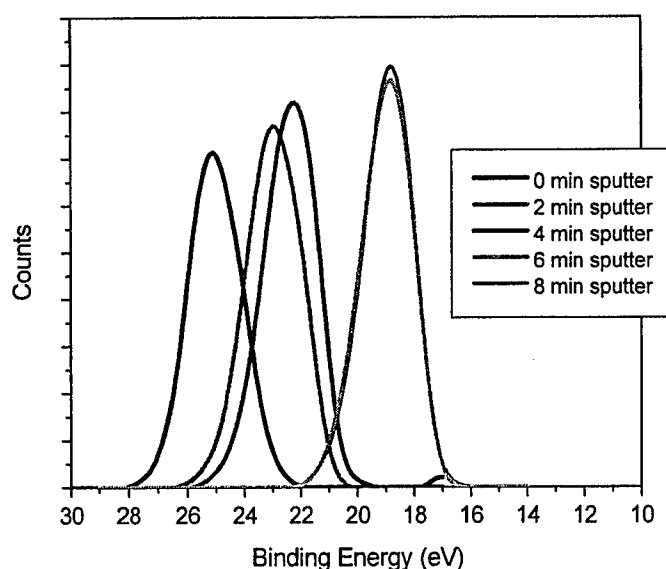


Figure 4.1.3. Ga 3d XPS spectra taken from GaN surface after 25 min. exposure to UV ozone as a function of sputter time. Depth was determined by monitoring the O 1s signal.

One concern which arose regarding the passivation scheme used in this work, was an apparent increase in the isolation current. It was found that the UV exposure increased the isolation current by as much as a factor of a thousand. This phenomena was studied and it was found that after roughly three days, the isolation current returned to pre-ozone levels. This indicates that the cause for the increase in isolation current is traps in the GaN buffer, which empty upon exposure to the UV in the ozone system. An XPS study of this shows the same. A GaN terminated HEMT structure surface spectra was collected, shown in Figure 4.1.5. This sample was then exposed to UV-ozone for 25 minutes and measured. The spectra shifted 5eV, as is typically seen. The sample was then held for three days in ultra high vacuum. The surface charge was then measured to be approximately 3.5eV, indicating that the traps had refilled over time. The surface still held charge and that charge was removed by sputtering the oxide. Thus it does not appear that the UV exposure presents any long term degradation problem. Further improvement of the GaN buffer will most likely eliminate even the short term leakage.

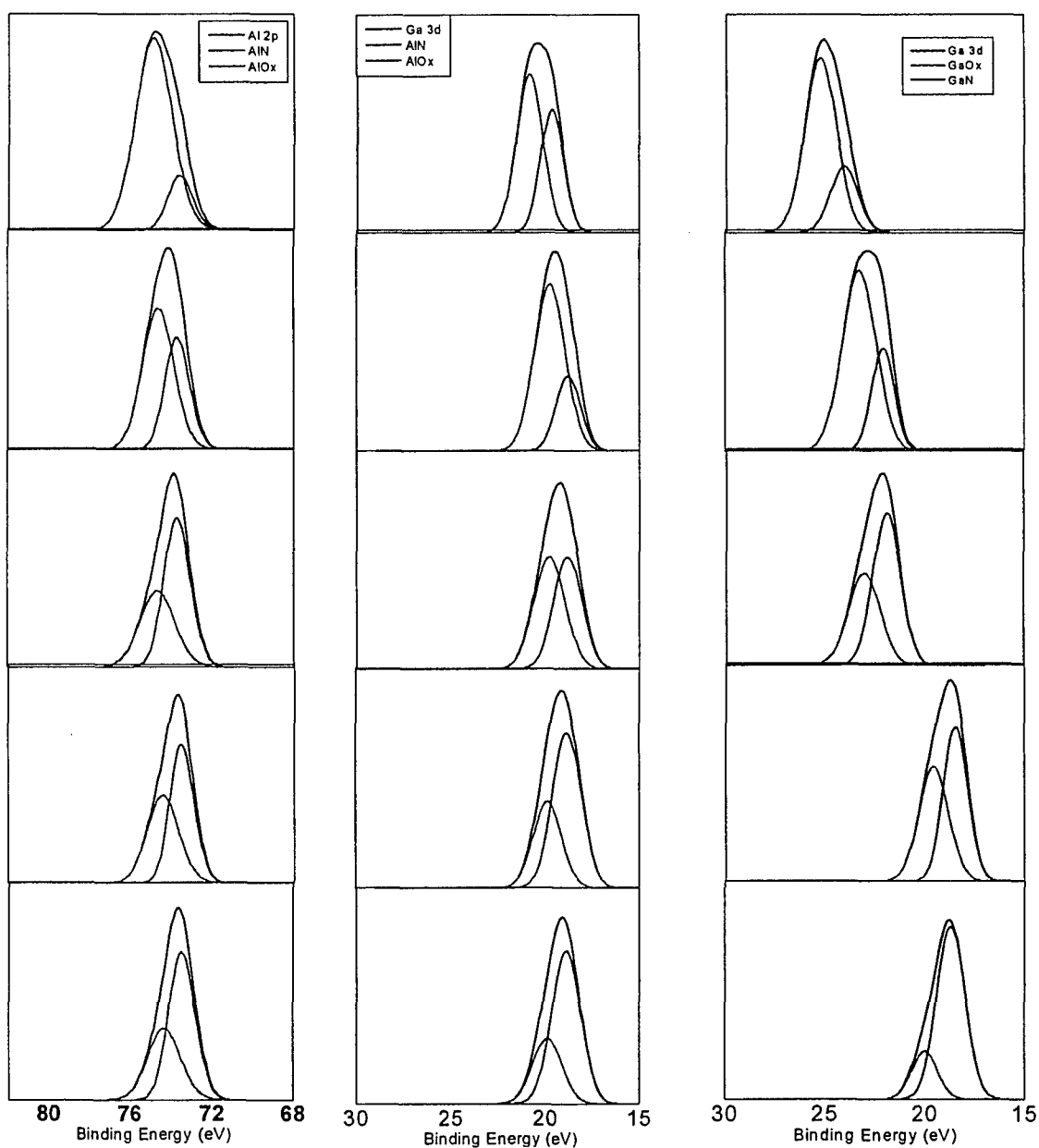


Figure 4.1.4. XPS spectra of AlGaIn capped HEMT with $X_{Al} \sim 25\%$ taken at sputter intervals of two minutes from no sputter (top) to 8 min. of sputter time (bottom). The Al 2p spectra is shown at left and the Ga 3d spectra is shown in the center. For comparison the Ga 3d spectra taken from a GaN capped HEMT is shown at right. Notice the decrease in the AlO_x portion (corresponding with sputter time) and the minor shift in the Al 2p signal indicative of minimal, ~ 1 eV, surface charge.

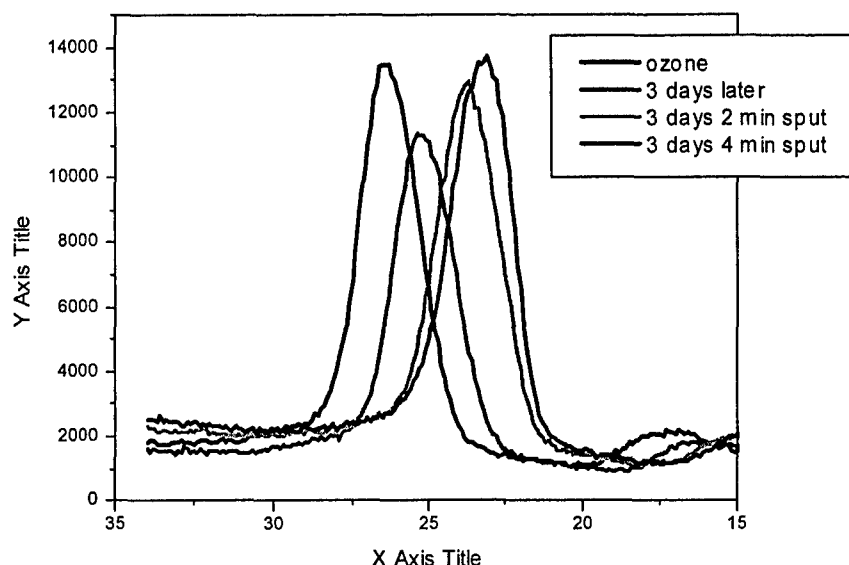


Figure 4.1.5. XPS spectra of oxide/GaN surface.

4.1.2 Effect of UV Ozone exposure on SiNx passivation of AlGaN capped HEMTs

In recent experiments, SiNx passivation has been found to cause degradation in the effective resistance between mesa-isolated devices. It is desirable to find an efficient means to limit this degradation in the process of SiNx passivation because SiNx is currently one of the most readily available and established means used to passivate GaN HEMT devices [1, 2]. One approach to improve SiNx passivation is through the use of UV-ozone exposure of the GaN surface to form a protective oxide under the nitride layer. As discussed in the previous section, UV-ozone exposure is the primary cleaning step in the oxide passivation scheme being developed under this program, thus understanding the role of the UV generated oxide is beneficial to non-nitride passivation schemes as well. In collaboration with N. Moser, R. C. Fitch, A. Crespo, J. K. Gillespie, G.H. Jessen, and G. D. Via in the Sensors Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base we have investigated the effect of UV exposure on inter-device isolation currents, breakdown voltages, and DC and RF device characteristics.

The HEMT structure for this experiment consisted of a 230 Å $\text{Al}_3\text{Ga}_7\text{N}$ unintentionally doped contact layer with a 2 μm GaN buffer layer on a sapphire substrate (initial experiments also indicate results are typical for SiC substrates as well). The initial 2" wafer was processed through mesa isolation, ohmic, and gate, and then sawed into 9 smaller samples each passivated using different techniques. The mesa portion of processing consisted of a lithography step followed by a ~1000 Å inductively coupled plasma (ICP) mesa etch using a Unaxis SLR 790 ICP etching tool. The etched area outside the mesa was then measured to insure good isolation on a manual probe station. DC leakage current was shown to be less than 100nA at 400V bias. Ohmic processing consisted of ohmic lithography followed by standard Ti/Al/Ni/Au (350/2333/500/200 Å) ohmic metal deposition in a Temescal BJD-300 metal evaporator. Ohmic liftoff was performed, and the ohmic metal was annealed at 850° C for 30 seconds in a STEAG SHS-100 Rapid Thermal Annealing (RTA) system with a constant N_2 flow. Process control monitor (PCM) measurements were taken with a Kiethley 450 24-pin probe card

following ohmic anneal. Gate processing began with a lithography step followed by standard Ni/Au (200/2800 Å) gate metal deposition using a Temescal BJD-300 metal evaporator. Following deposition, gate metal liftoff was performed and PCM and DC/RF measurements were taken using a Kiethley 450 24-pin probe card for PCM and an HP4142/HP8510 combination with cascade probes for DC/RF. The 2" wafer was then sawed into 9 individual samples. The samples were all immediately retested for PCM results to insure no adverse effects from the sawing.

Two of the samples received UV-ozone treatment followed by SiNx passivation, one sample received standard SiNx passivation with no UV-ozone, and a fourth sample received no passivation at all as a control. The two samples receiving UV-ozone pre-treated SiNx passivation were pre-treated using a UV-Cleaner model 42-220 UV treatment system for 25 minutes. The samples were then passivated using the Air Force Research Lab and University of Florida Unaxis 790 plasma enhanced chemical vapor deposition (PECVD) systems. The sample passivated without UV-ozone pre-treatment was passivated using the Air Force Research Lab Unaxis 790 PECVD. Contact pads were opened following passivation using a lithography step and a Unaxis Batch 80 Reactive Ion Etching (RIE) system. The samples were then put through a final test of both PCM and DC/RF characteristics.

Inter-device isolation results

Inter-device isolation parameters were measured on an isolation structure consisting of two 50x50 µm mesas separated by a 10 µm mesa gap. Breakdown Voltage measurements were recorded as the mesa-to-mesa voltage measured for a cross-gap forced current of 100 nA (the maximum forcing voltage for the tester was 60 V). Isolation current measurements were recorded as the amount of cross-gap current flow for a 50 V bias from mesa to mesa. As seen in Figure 4.1.6, the UV-ozone pre-treated samples exhibited a much higher breakdown voltage. Without the UV-ozone pre-treatment before SiNx PECVD, inter-device breakdown voltages fell from a test max of 60 V before passivation to ~5 V after SiNx passivation. The breakdown voltage values with UV-ozone pre-treatment, however, remained at ~58 V after SiNx passivation.

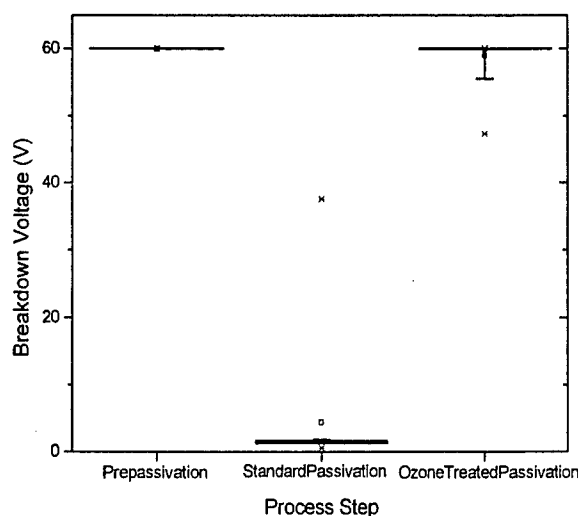


Fig 4.1.6: Breakdown Voltages for Standard and UV-Ozone Treated SiNx Passivation

Similarly, in Figure 4.1.7, the UV-ozone pre-treated samples exhibited much lower isolation current than the standard SiNx passivation process. Standard SiNx passivation without UV-ozone caused an increase from values on the order of 10^{-9} A before passivation to values on the order of 10^{-6} A after passivation. SiNx passivation that was preceded by UV-ozone treatment, however, caused an isolation current measured on the order of only 10^{-8} A, two orders of magnitude better than the untreated passivation.

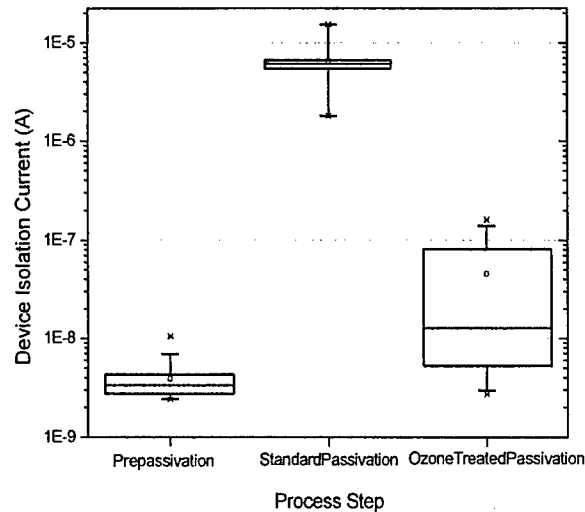


Fig 4.1.7: Device Isolation Current for Standard and UV-ozone Treated SiNx Passivation

Characterization of uv-ozone treated surface

In order to characterize the effects of the UV-ozone treatment on the samples before deposition of SiNx, X-ray Photo Spectroscopy (XPS) and transmission electron microscopy (TEM) measurements were taken. The TEM measurements were taken using a JEOL 2010 TEM employing a field emission gun as electron source. The XPS measurements were obtained using an XPS/ESCA Perkin-Elmer PHI 5100 System with an Mg anode x-ray source at 15 KV.

TEM measurements revealed a UV-ozone grown oxide (GaO_x) between 15 and 25 Å. This was the expected result of the UV-ozone treatment on the samples. The produced oxide is intended to provide a thin buffer layer between the SiNx and the AlGaIn surface of the samples. Many sources have been credited for degradation of device characteristics after passivation, among these are piezoelectric stress caused by the SiNx on the AlGaIn surface, chemical process between the AlGaIn and Si in the SiNx, and PECVD damage of the surface by SiNx passivation processes [2]. The oxide layer produced by the UV-ozone may provide a method to reduce all of these effects, however, the actual cause of degradation is currently still being investigated.

Immediately following UV-ozone treatment, device isolation current was found to increase a small amount. However, after being exposed to air for 2-3 days the samples recovered and were actually sometimes better (by a small amount) than the samples without UV-ozone treatment (Figure 4.1.8). As discussed in the previous section, XPS

results indicate that this initial increase in isolation current is more likely the result of an excitation under UV exposure of deep trap states in the GaN buffer.

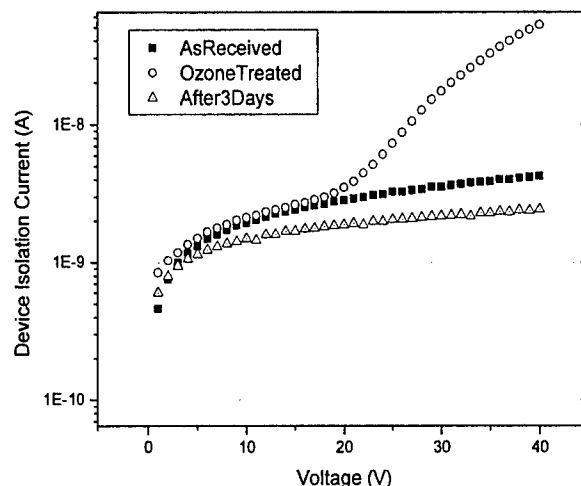


Figure 4.1.8: Change in Isolation Current after UV-ozone Pre-Treatment

Dc/rf and pcm passivation effectiveness results

In order to ensure the effectiveness of the UV-ozone treated SiNx passivation, DC/RF and PCM measurements for samples with and without UV exposure were compared. The UV-ozone pre-treated passivation shows no significant differences in its ability to promote the desired device performance results. DC/RF measurements were taken from a designed 1.0 μ m (measured 1.0 μ m) gate length 300 (2x150) μ m gate periphery device. In Figures 4.1.9 and 4.1.10 transconductance (G_m) curves of both an ozone treated passivation and a standard SiNx passivation are shown in comparison to the pre-passivated devices. The gate voltage was first swept forward and then in reverse. The dispersion effects (difference between the forward and reverse gate voltage sweeps) were observed to be drastically reduced for both the standard SiNx passivation and the UV-ozone pre-treated SiNx passivation.

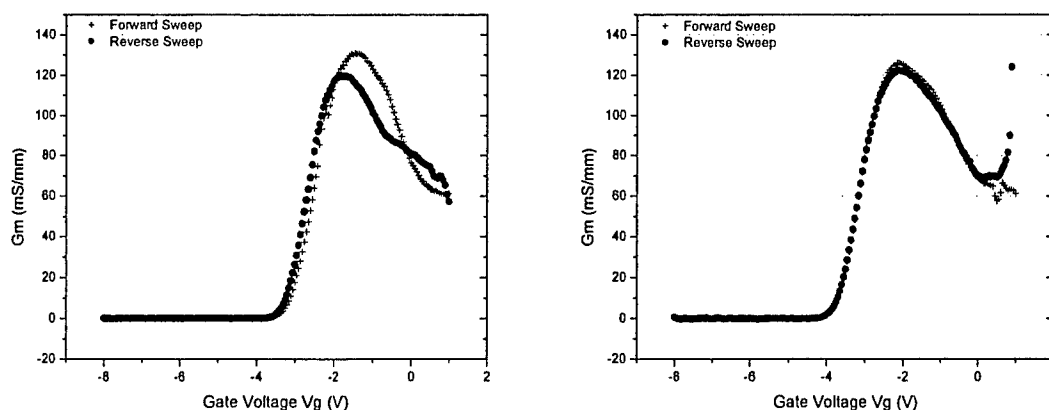


Fig 4.1.9: Forward and Reverse G_m Sweeps for Pre Passivation (Left) and Post Standard Passivation (Right)

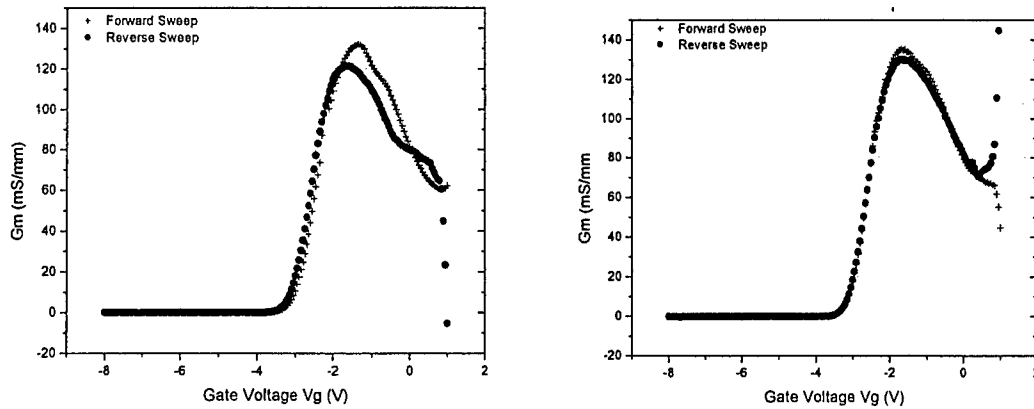


Fig 4.1.10: Forward and Reverse G_m Sweeps for Pre Passivation (Left) and UV-ozone Treated Passivation (Right)

In Figures 4.1.11 and 4.1.12 IV curves for both a UV-ozone treated passivation and a standard SiNx passivation are shown. In both cases it is seen that the peak drain current produced by the device increased after passivation. A comparison of average cutoff frequency (f_T) for unpassivated devices, standard SiNx passivated devices, and UV-ozone treated SiNx passivated devices also demonstrated no discrepancies in the UV-ozone pre-treatment process. The two passivation schemes both improve the f_T values slightly, but UV-ozone treated passivation is actually shown to be slightly better. For the standard passivation sample, f_T was found to rise from an average of 7.48 GHz before passivation to 7.54 GHz after passivation. For the UV-ozone pre-treated passivation sample, f_T was found to rise from an average of 7.51 GHz before passivation to 8.28 GHz after passivation.

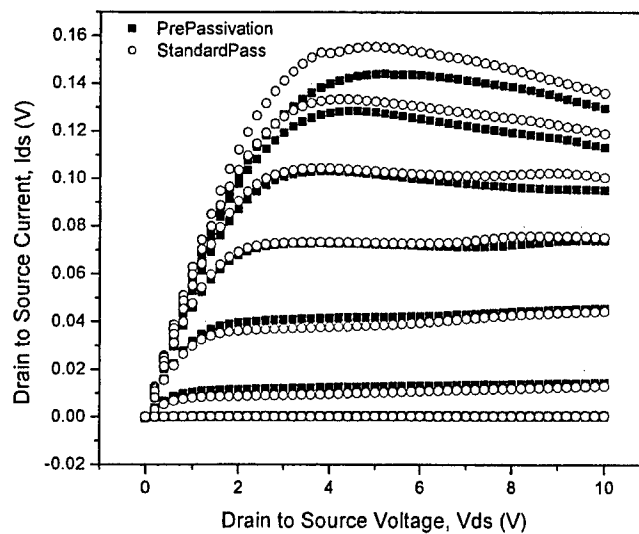


Figure 4.1.11: IV Curves Before Passivation and After Standard Passivation

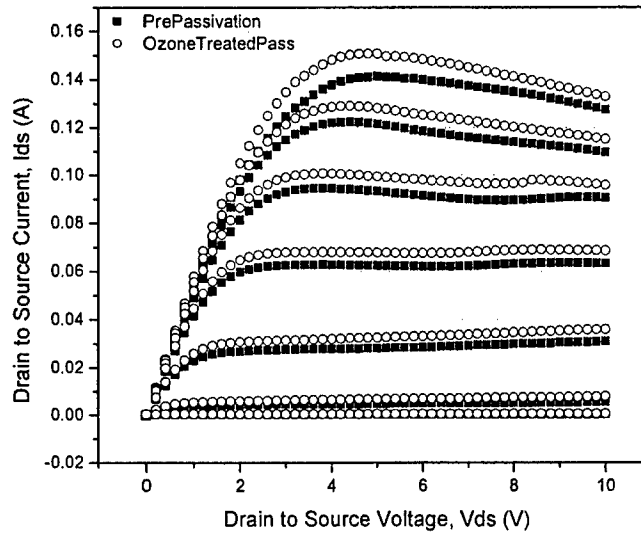


Figure 4.1.12: IV Curves Before Passivation and After UV-ozone Treated Passivation

Because of significant benefits in the inter-device isolation characteristics, UV-ozone treatment is an efficient and effective step to precede a standard SiNx process. The device isolation characteristics are still not ideal and other forms of passivation appear to provide better results [2,3,4-6]. However, since SiNx is an established passivation technique, this method is often used to reduce surface/interface leakage. The mechanism for inter-device leakage is still unclear. The material beneath the SiNx /buffer interface may still be a source of leakage.

4.1.3 Effect of Free Standing GaN Substrates on DC Characteristics of AlGaIn/GaN Heterostructure Field-Effect Transistors

In order to investigate the source of the defects responsible for the current collapse phenomenon, we explored the effects of using free-standing GaN substrates in place of sapphire or SiC. To date, only a few reports have appeared on the characteristics of HFETs grown on bulk GaN substrates [7,8]. These devices exhibited better linearity of transconductance and lower gate leakage relative to heteroepitaxial devices [7], but little information is available regarding the effect of GaN substrates on current collapse. Zhang et al. have shown that there is a strong correlation of the device performance with the presence of dislocations with screw components that terminate on the surface and that these can degrade the effectiveness of SiNx surface passivation [9]. The lower dislocation density in structures grown on free-standing substrates as measured by a variety of techniques such as transmission electron microscope, etch pit counting and atomic force microscopy should lead to a reduced current collapse effect if the conventional wisdom conceiving the role of defects is correct [10-12].

The nominally undoped, n-type free-standing GaN substrates used in this study were ~200 μm thick and were grown by high-rate vapor phase epitaxy on c-plane Al_2O_3 substrates and removed by differential heating from a laser beam [13-16]. The same

HFET structures were grown by metal organic chemical vapor deposition (MOCVD) on both the GaN substrates and c-plane sapphire. The structure consisted of a 3 μm thick, undoped GaN buffer and 40nm unintentionally doped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layer. Device isolation was performed with Cl_2/Ar Inductively Coupled Plasma mesa etching. Ohmic contacts were formed by lift-off of e-beam deposited Ti/Al/Pt/Au (20 nm/100 nm/40 nm/80 nm) that was subsequently annealed at 850 $^\circ\text{C}$ for 45s under a flowing N_2 ambient. Schottky gates ($1 \times 200 \mu\text{m}$) of e-beam deposited Pt/Au were also patterned by lift-off. The characteristics of devices on bulk GaN and sapphire substrates were measured in dc and pulsed mode using an Agilent 4156C parameter analyzer for dc mode and a pulse generator, dc power supply and oscilloscope for the pulsed measurements.

Unpassivated devices

Figure 4.1.13 shows the drain-source current (I_{DS}) as a function of drain-source voltage (V_{DS}) for both the GaN substrate HFETs (top) and those grown on sapphire (bottom). The homoepitaxial HFETs show a slight lower knee voltage and higher output resistance than the heteroepitaxial devices, and these attribute from better mobility in the 2DEG and less leakage current in the GaN buffer layer, respectively. The peak saturation currents are similar for both types of HFETs at $0.45 \text{ A} \cdot \text{mm}^{-1}$, which is expected given that the sheet resistance and specific contact resistance were within 10% for the two structures. When pushed to higher drain-source voltages, the GaN substrate HFETs showed less negative slope in the current-voltage characteristics, as shown in Figure 4.1.14. This is generally accepted to be an indication of less self-heating and is expected given the higher thermal conductivity ($\sim 1.5 \text{ Wmm}^{-1}$) for GaN relative to Al_2O_3 ($\sim 0.5 \text{ Wmm}^{-1}$).

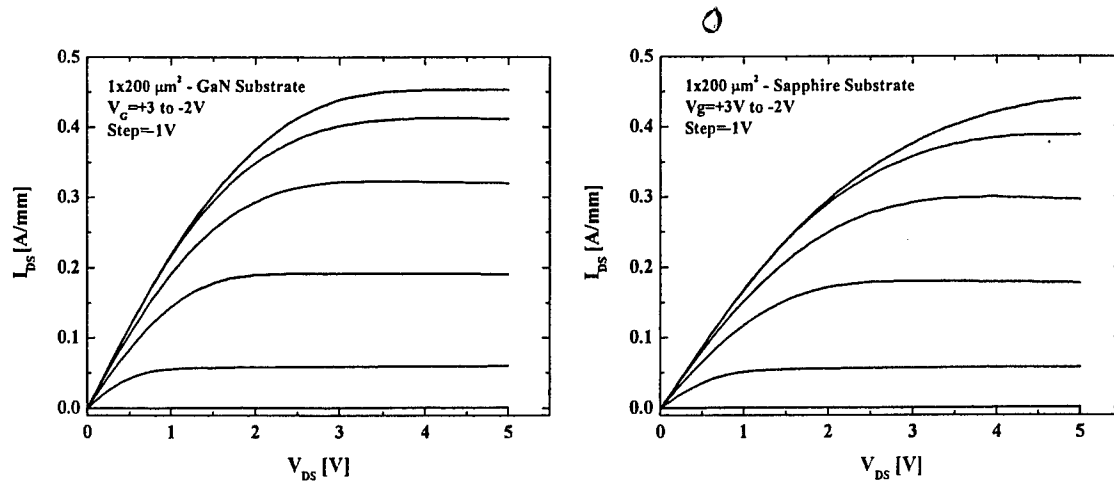


Figure 4.1.13. IDS-VDS characteristics for $1 \times 200 \mu\text{m}^2$ HFETs grown on GaN substrate (left) or sapphire substrate (right).

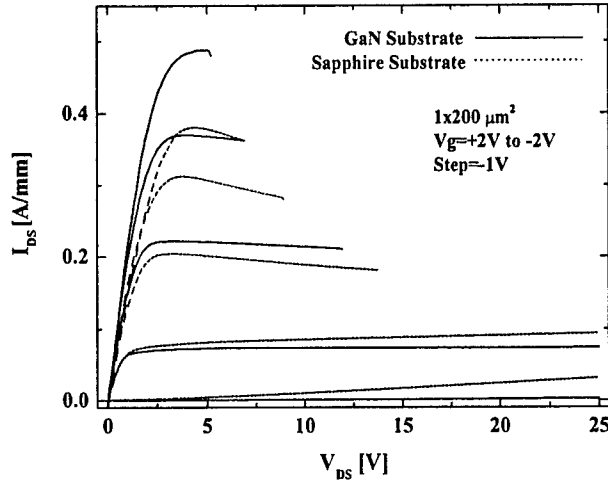


Figure 4.1.14. I_{DS} - V_{DS} characteristics for high bias conditions, showing less self-heating for HFETs grown on GaN substrates.

The transconductance of the homoepitaxial HFETs was higher compared to the heteroepitaxial devices (~ 140 mS/mm cf. 128 mS/mm) with a slight shift (~ 0.25 V) to more negative voltage in the latter case, as shown in Figure 4.1.15. This is due to better gate modulation of the HFET on the GaN substrate. The threshold voltages are similar in both types of device and indicate that the sheet electron densities are similar in both cases. The devices on sapphire are expected to be under tensile strain because of the lattice mismatch, whereas the HFETs in GaN should be essentially strain-free.

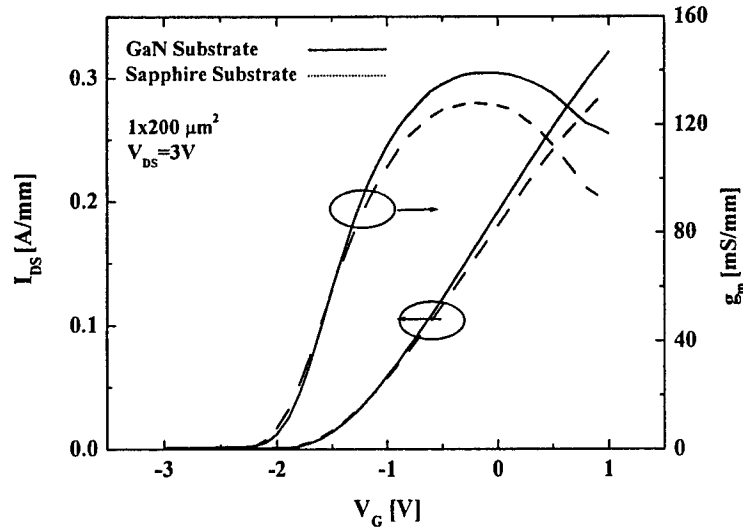


Figure 4.1.15. Transfer characteristics for HFETs grown either on GaN or sapphire substrates.

To investigate the effects of surface states on the current in the HFETs, gate lag measurements were performed. Figure 4.1.16 shows the drain current response of both types of devices to a pulsed gate-source voltage, along with the corresponding dc results. The gate voltage was pulsed from 0 to -3 V of 0.1 MHz with a 10% duty cycle. The HFETs on sapphire show a decrease of $> 50\%$ in drain-source current. This decrease in

current is a result of the presence of surface states in the gate-drain region, which create a virtual gate that depletes the channel, and reduces the output power at high biases. This phenomenon can be effectively mitigated in our heteroepitaxial devices by use of thin surface passivation oxides (Sc_2O_3 and MgO), which provides strong evidence for the role of surface traps that have been observed by capacitance spectroscopy. Figure 4.1.16 (left) shows that the homoepitaxial HFETs show a much reduced degree of current degradation, with $\leq 10\%$ difference between pulsed and dc measurements. This suggests that the majority of the surface states in heteroepitaxial devices must be associated with dislocations and other extended defects present as a result of the large mismatch in the $\text{AlGaIn}/\text{GaIn}/\text{Al}_2\text{O}_3$ system. Additional data is shown in Figure 4.1.17, where the V_{DS} was fixed at a low enough voltage (3 V) to avoid self-heating and the drain-source current was measured as the gate voltage was switched from -3 V to the value shown in the x-axis. Once again there is much less degradation in I_{DS} in the homoepitaxial HFETs compared to the heteroepitaxial devices, suggesting that the surface states must be associated with the higher defect density in the nitride layers grown on Al_2O_3 .

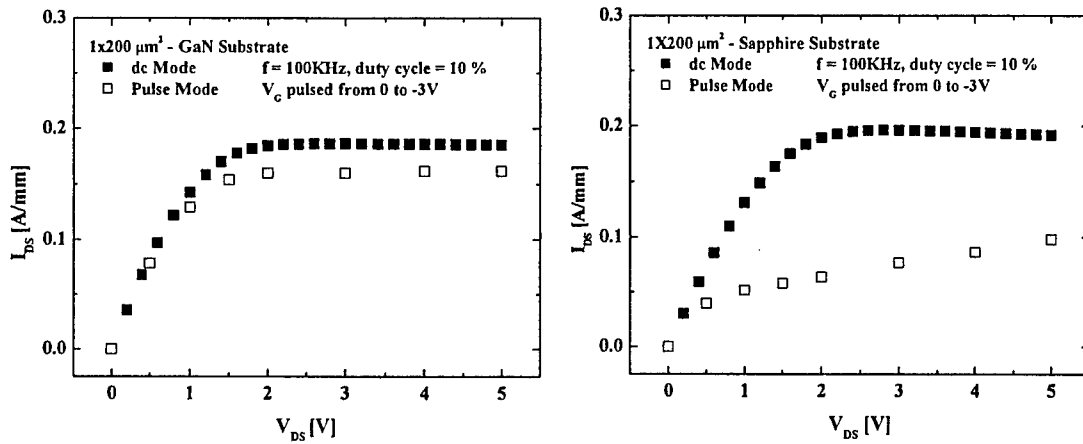


Figure 4.1.16. Gate lag measurement of HFETs with gate voltage pulsed from 0 to -3 V. The devices were grown either on GaN (left) or sapphire (right) substrates.

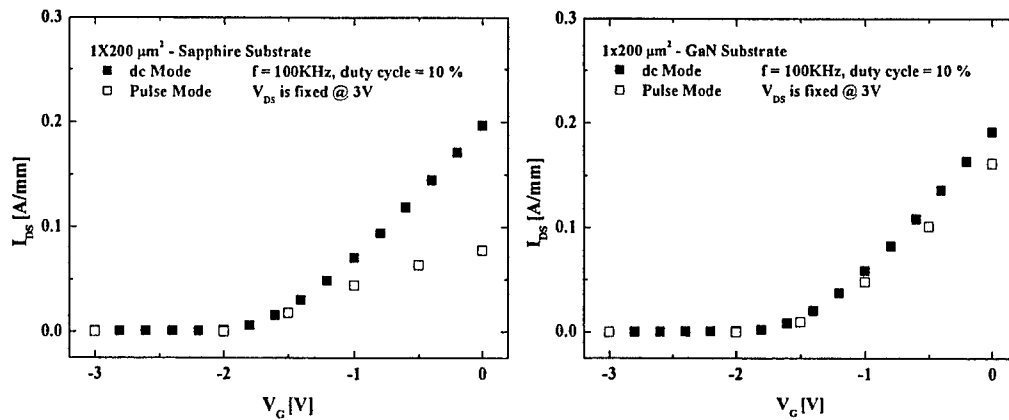


Figure 4.1.17. Gate lag measurement of HFETs with gate voltage pulsed from -3 V to the value shown on the x-axis. The devices were grown either on GaN (left) or sapphire (right) substrates.

Passivated devices

Figure 4.1.18 shows transfer characteristics of the unpassivated (at left) and Sc_2O_3 -passivated (at right) devices on both the Al_2O_3 and GaN substrates. The Sc_2O_3 passivation causes the threshold voltage of the heteroepitaxial HFETs to shift to more negative voltage, indicating an increase in effective channel charge density. This is consistent with a reduction in surface depletion through passivation of surface states in the gate-drain region. By sharp contrast, the homoepitaxial devices show little change, indicating that they did not suffer as much initially from the presence of these surface states.

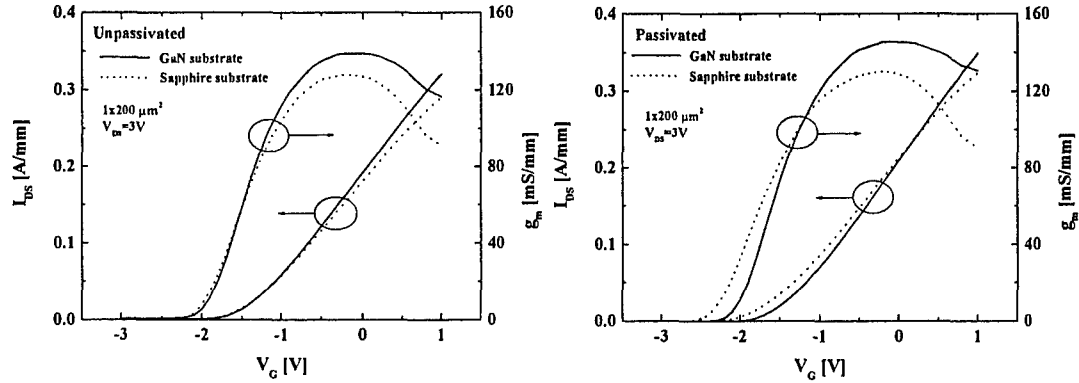


Figure 4.1.18. Transfer characteristics for HFETs on either GaN or Al_2O_3 substrates before (at left) and after (at right) Sc_2O_3 passivation.

Figure 4.1.19 shows the drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) characteristics from both types of devices before and after passivation. Both types of devices show higher drain-source current after Sc_2O_3 passivation due to a reduction of electron accumulation into surface traps associated with dislocations and other defects. Figure 4.1.20 shows the normalized I_{DS} as a function of V_{DS} for both pulsed and dc measurements on both types of devices. Note that in the HFETs on Al_2O_3 (at left), there is a large difference between the dc and pulsed drain current in unpassivated devices. The Sc_2O_3 passivation mitigates most of this current degradation. By contrast, the HFETs on GaN show a much lower initial amount of gate current lag and therefore a smaller improvement upon passivation.

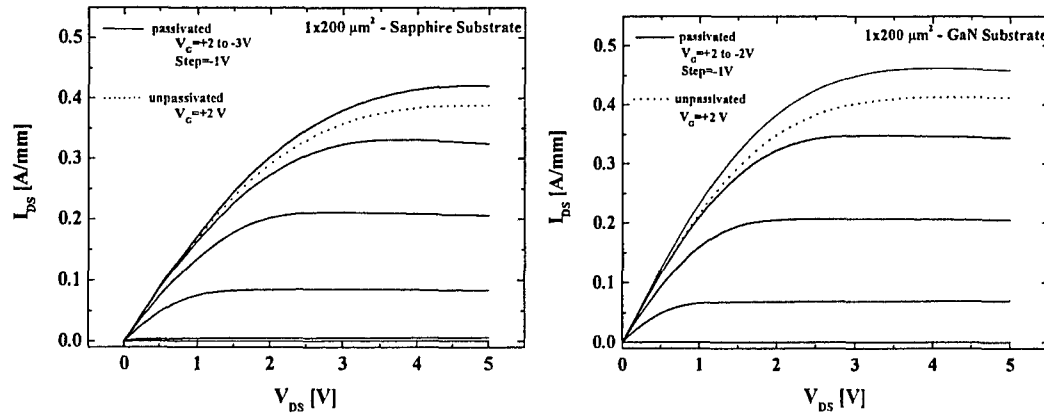


Figure 4.1.19. $I_{\text{DS}}-V_{\text{DS}}$ characteristics for passivated and unpassivated HFETs on Al_2O_3 (at left) or GaN (at right) substrates.

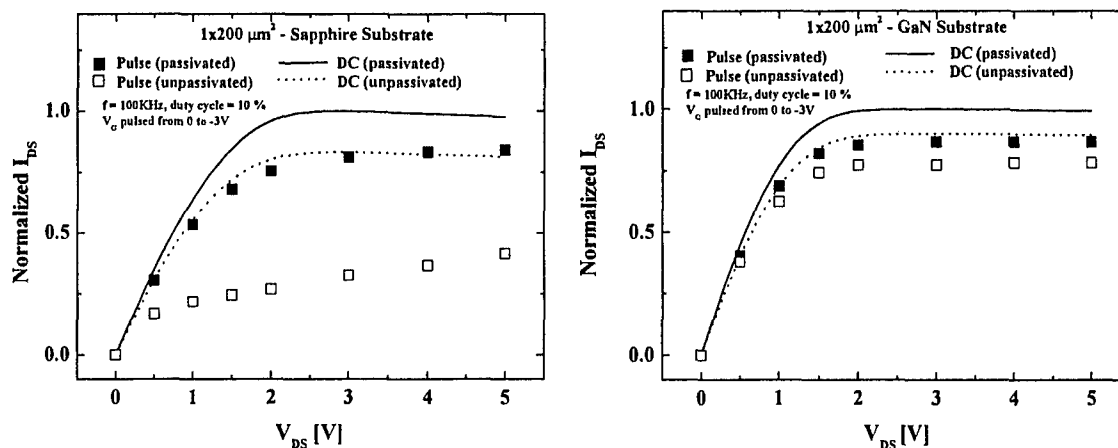


Figure 4.1.20. Gate lag measurement before and after passivation for HFETs on Al_2O_3 (at left) or GaN (at right) substrates. The gate voltage was pulsed from 0 to -3 V.

Similar conclusion can be drawn from the data of Figure 4.1.21, which shows the normalized I_{DS} when V_{DS} is fixed at 3 V and V_G is pulsed from -3 V to the value shown on the x-axis. The large difference between dc and pulsed drain current in the unpassivated HFETs on Al_2O_3 is consistent with the presence of a high density of surface traps that deplete the channel. This effect is much less pronounced in the case of HFETs on GaN and suggests the reduced defect density in their structures is the cause of the improved device performance.

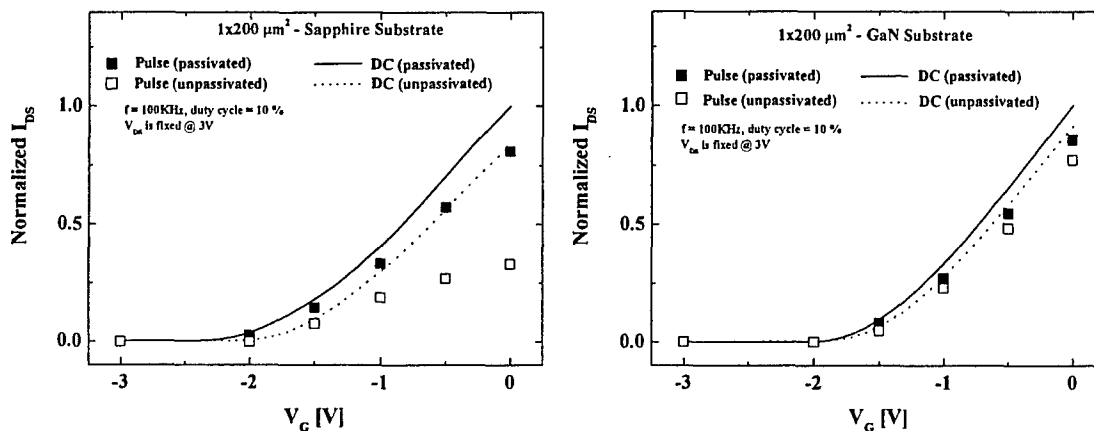


Figure 4.1.21. Gate lag measurement before and after passivation for HFETs on Al_2O_3 (at left) or GaN (at right) substrates. The gate voltage was pulsed from -3 V to the value shown on the x-axis.

4.1.4 X-TEM of AlGaIn/GaN HEMT devices

In collaboration with Bob Fitch (WPAFB), investigation of processed HEMT devices via cross-section TEM is being preformed in order to correlate defect densities and types with device failure modes. The following areas are being investigated: gate

metal/AlGaN interface, AlGaN layer uniformity and source(or drain) metal/AlGaN interface. This type of device study requires that the area of interest be removed from the wafer by a Focused Ion Beam (FIB) technique. Under this program we are developing a recipe for FIB fabrication of XTEM samples from processed HEMT devices. Extreme care must be taken in this procedure to prevent damage to the area of interest. Initial images of these devices, Figure 4.1.22, show the SiNx passivation (applied by WPAFB) to be very uniform and contiguous beneath the e-beam defined T-gate. Common screw dislocations are seen within the device as well as a strained layer beneath the AlGaN layer.

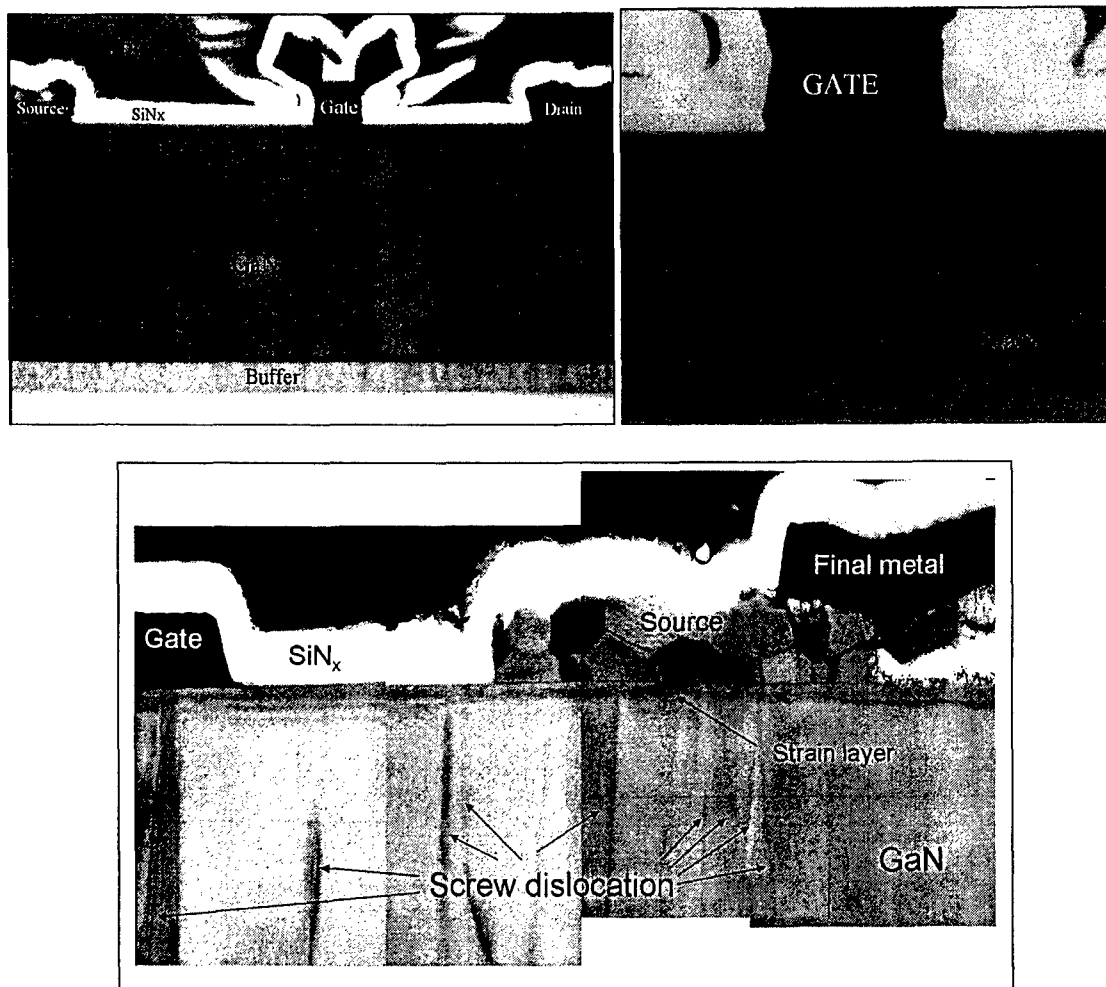


Figure 4.1.22. XTEM micrographs of processed AlGaN capped HEMTs.

4.1.5 Low temperature GaN growth for AlGaN post-process capping

From our previous studies on the AlGaN and GaN surfaces, it was observed that the ozone treatment produces a surface oxide layer that is approximately four times thicker than the native oxide layer. The ozone induced oxide layer on AlGaN has similar properties to the native oxide layer in that the X-ray Photoelectron Spectroscopy (XPS)

measurement does not induce a positive surface charge from electrons escaping the surface. This suggests that the AlGaO_x oxide is somewhat conductive. By contrast, the ozone induced oxide layer on GaN has properties that are different from those of the native oxide. Here, the XPS measurement induces a net positive charge on the surface by escaping electrons not being replenished from the substrate due to the GaOx being more insulating. This insulating GaOx layer plays a major role in the ability to passivate the surface on fabricated HEMT devices. As seen from our previous work, HEMTs that have thin GaN caps (2-3nm) over the final AlGaIn/GaN structure have a higher pulse current recovery (90-95%) compared to HEMT structures without the GaN cap (80-85%) after passivation. Also, as the Al concentration levels rise from the typical 20%-23% to the level of 30%-35%, the top AlGaIn layer reactivity with ambient atmosphere increases severely. This leads to reduced passivation efficiency from the deposited oxides as this AlGaO_x layer forms more readily and is most likely thicker, due to the higher reactivity of aluminum.

In light of these results, we believe that the GaN surface and not the AlGaIn surface will provide a better ozone induced oxide for surface passivation. Since the typical AlGaIn/GaN HEMT structure is not terminated with GaN, we propose to deposit a thin (2-3 nm) low temperature (300°C) GaN layer via MBE over the final HEMT structure. This layer would then be transformed into GaOx via the UV-ozone treatment prior to passivation oxide deposition. In this reporting period we have investigated the low temperature growth of GaN. Initial growth of GaN at 300°C was performed on Si substrates using a gallium cell temperature of 730°C and nitrogen pressure of $2.7\text{E-}5$ Torr. From depth profile Auger Electron Spectroscopy (AES), it was observed that a continuous film of GaN was deposited. This film was approximately 4.0nm thick estimated by the depth profile, shown in Figure 4.1.23. The film is clearly continuous due to the lack of a silicon signal at the surface. The Ga:N ratio observed in the AES surface scan is consistent with stoichiometric GaN. From in-situ Reflection High Energy Electron Diffraction (RHEED), the GaN was polycrystalline as expected.

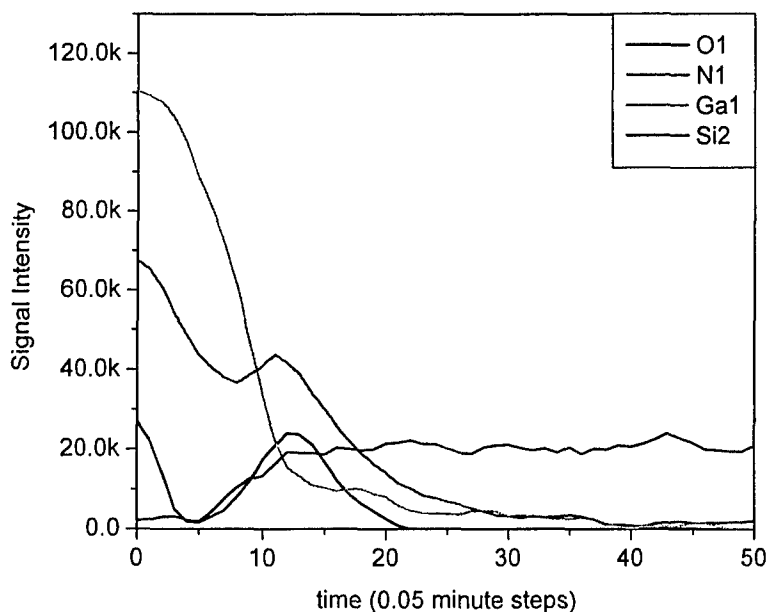


Figure 4.1.23. AES depth profile of GaN grown at 300°C on Si wafer.

Further growth experiments were carried out employing AlN as a marker layer for the thin, low temperature growth of GaN. A 200nm layer of AlN was grown at 900°C prior to the GaN growth at 300°C in the same MBE chamber. The same conditions were used for the GaN growth as previously used for the GaN on Si growth. Layer thicknesses were estimated at 3.7nm, shown in Figure 4.1.24. These samples were exposed to our UV-ozone treatment and it was found by AES that the ozone consumed nearly all of the deposited GaN. If the growth time is reduced, a thinner film of GaN can be deposited and the entire GaN layer consumed into GaOx, thus creating a very thin, insulating surface for improved passivation.

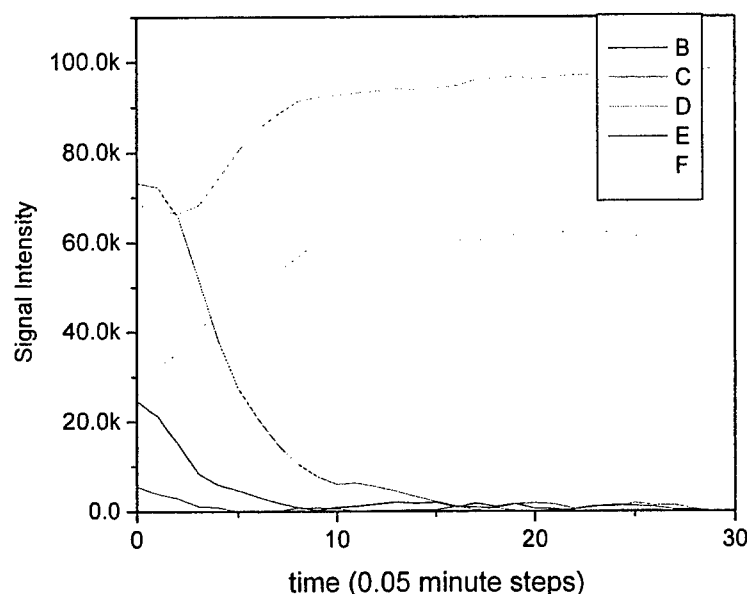


Figure 4.1.24. AES depth profile of GaN grown at 300°C on AlN buffer. Oxygen is due to formation of surface oxide upon exposure to air.

4.1.6 UV-ozone as a screening method for HEMT devices

UV-ozone exposure has also been shown to be effective as a screening method for evaluation of HEMT device material. From numerous passivation experiments and device testing, a link between nitride material/device quality and the effect of UV-ozone exposure on the HEMT device performance has been observed. Typically in high quality HEMT material, it is noticed that the pulsed V_{ds} - I_{ds} plot will slightly increase immediately after the UV treatment. After three days, the pulsed V_{ds} - I_{ds} increases further, similar to the trend observed with the isolation current, as shown in Figure 4.1.25. This device showed further improvement after the dielectric passivation was deposited. When this same procedure is preformed on a HEMT device fabricated from poor quality material, exposure to the UV-ozone produces little to no immediate effect and the three day test improves only slightly. On a few occasions, the pulsed V_{ds} - I_{ds}

decreased after the UV-ozone treatment and never recovered after the three day period. This is due to a very large number of carrier traps in the nitride material that have a lifetime far greater than the three day recovery period. It is also interesting to note that the isolation current of these poorer material quality HEMT devices is still relatively good, remaining in the nA range. This indicates that the carrier traps are likely located within the AlGaIn and/or the AlGaIn/GaN interface region, within the top 35nm of the device structure. A simple test device structure can be designed and processed on as-grown wafers as a cursory exam to indicate if the nitride material quality is high enough to be processed into final HEMT structures.

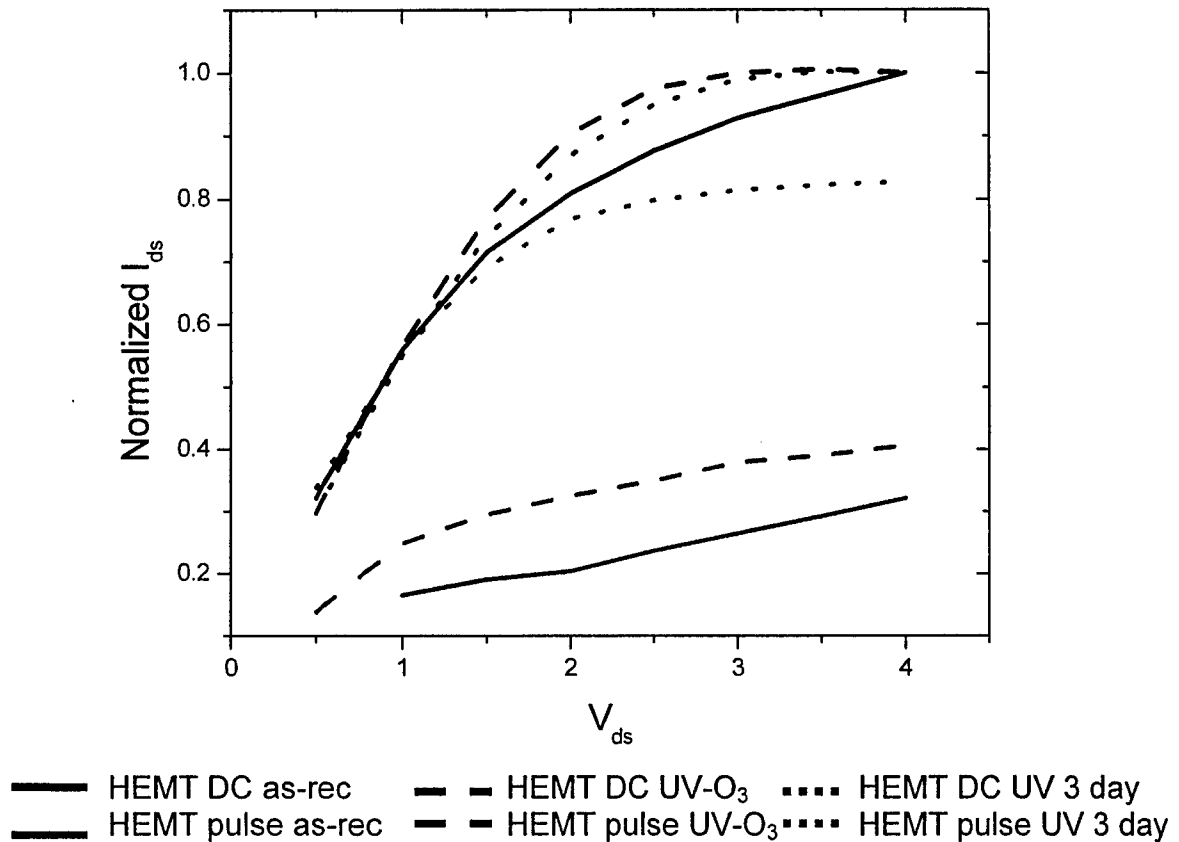


Figure 4.1.25. V_{ds} - I_{ds} of both pulsed mode (red plots) and dc mode (black plots) for a high quality HEMT device as-processed (straight lines), same device immediately after UV-ozone treatment (dashed lines), and 3 days after UV-ozone treatment (dotted lines).

4.1.7 UV-ozone effects on surface oxynitride composition

It has been determined from previous data that the UV-ozone treatment prior to deposition of the passivation dielectric provides for better device passivation and device-device isolation than without. It has become a reliable screening tool for determining the quality of the device epitaxy in terms of buffer traps and has lead us to believe that a GaN capping lay on the final AlGaIn/GaN HEMT structure, when exposed to the UV-ozone,

becomes more insulating than AlGaN under the same conditions. This GaN capping layer has become the trend for several nitride HEMT device groups.

From previous XPS studies, it has been determined that the UV-ozone process creates a mixed oxide-nitride layer on the GaN or the AlGaN surface. The exact chemical composition, diffusion rate of oxygen and its effects upon the subsequent passivation are still unknown. Figure 4.1.26 is an XPS depth profile of an as received HEMT structure. The oxygen signal is present at the surface from the native oxide film, then falls to a lower value in the depth. It appears that the aluminum is of the same concentration as the oxygen in the bulk film, this is an artifact due to the different sensitivities of the elements and was not corrected for in these plots.

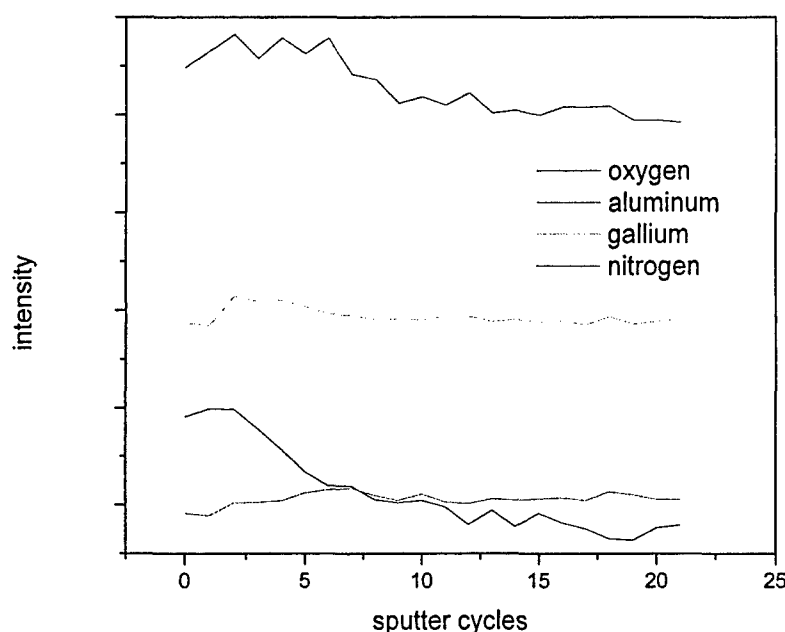


Figure 4.1.26 XPS depth profile of as-received HEMT structure.

The as-received HEMT structures were then exposed to UV-ozone for times of 12.5 minutes and 25 minutes, Figures 4.1.27 and 4.1.28 respectively. For the two UV-ozone exposures, it is clear that the surface stoichiometry (nitrogen vs. oxygen) is different. When the three samples are plotted together vs. oxygen concentration, figure 4.1.29, it becomes clear that the longer UV-ozone exposure leads to a higher oxygen content in the surface and that the oxygen diffusion depth is time independent. Therefore, the depth of nitride material consumed in the UV-ozone process is a constant over time, but the oxygen content is dependent upon the exposure time. A thermocouple was placed in the UV-ozone system and the highest temperature recorded for the exposure was approximately 50°C. This temperature is too low to provide adequate energy for the

oxidation process. The conversion of the surface nitride to an oxynitride film is therefore a surface reaction rate limited process and the active oxygen species does not diffuse more than a few monolayers into the nitride film. This allows for the composition of the oxynitride film to be altered without oxygen diffusing deeper into the HEMT structure. The composition of the oxynitride film and its effects on the passivation will be a topic for further study.

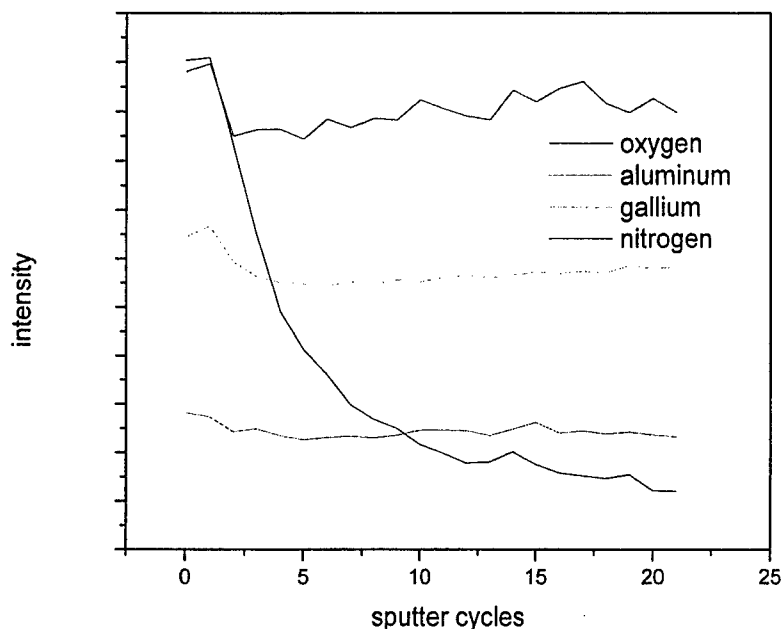


Figure 4.1.27 XPS depth profile of HEMT structure exposed to UV-ozone for 12.5 minutes.

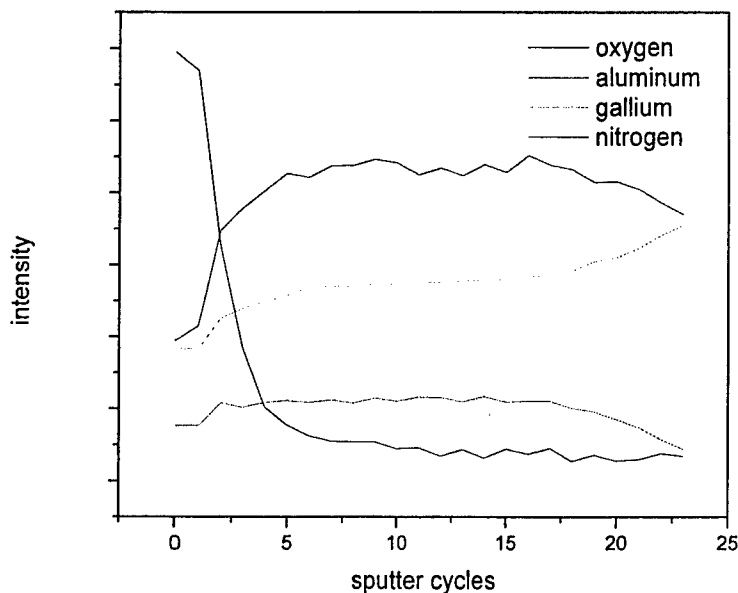


Figure 4.1.28 XPS depth profile of HEMT structure exposed to UV-ozone for 25 minutes.

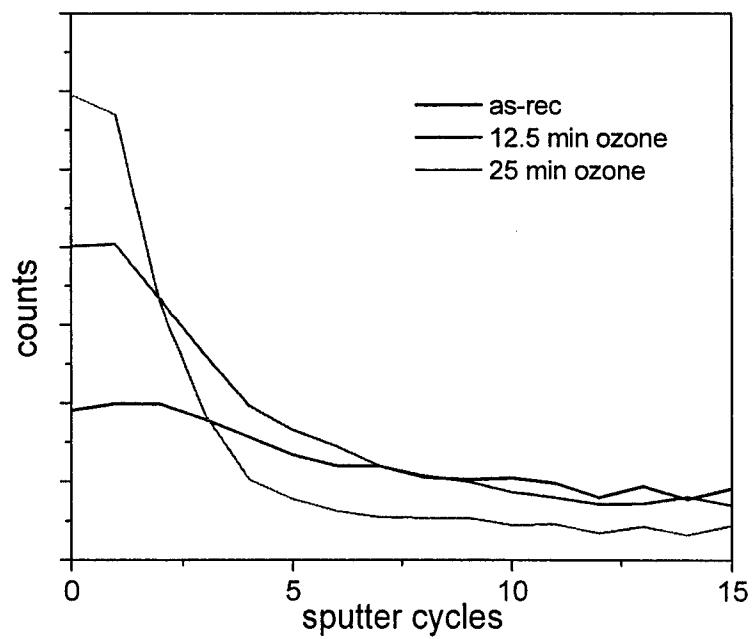


Figure 4.1.29 UV-ozone exposure time vs. oxygen concentration and depth.

4.2 Task 2: Improved Contact Metallization

Bob Fitch and colleagues at WPAFB have been investigating the use of Ir gates for improved thermal stability. Using HEMT devices supplied by WPAFB we have investigated the resistance of the Ir gates to degradation induced by the use of elevated temperatures prior to deposition of the low temperature oxide passivation layer. Unlike devices using conventional gate metals, we did not observe any degradation of the Ir even after heating to temperatures as high as 700°C. Such high temperatures should assist in the cleaning of the GaN surface and thus should result in better, more stable passivation. Further investigation into Ir as well as other alternative metallization schemes will continue in the second year of the program.

4.2.1 Thermal stability of Ir gates and final metal

The in-situ cleaning process used prior to dielectric deposition is critical to formation of a clean interface. High temperature thermal annealing/cleaning of the GaN surface is generally required to obtain a high quality interface. From other experiments we have learned that the highest quality oxide/nitride interfaces are obtained by employing a 700°C thermal anneal in vacuum prior to oxide deposition. This process produces the lowest density of interface traps due to the cleaner interface. . Currently, we have limited our pre-deposition thermal anneal to 300°C to avoid damage to the gate metal and final metal. We have observed that above this temperature, in a ultra-high vacuum environment, the metal is severely damaged and in some cases delaminated, Figure 4.2.1. It can be clearly seen that the metal begins to degrade even at a low temperature of 400°C.

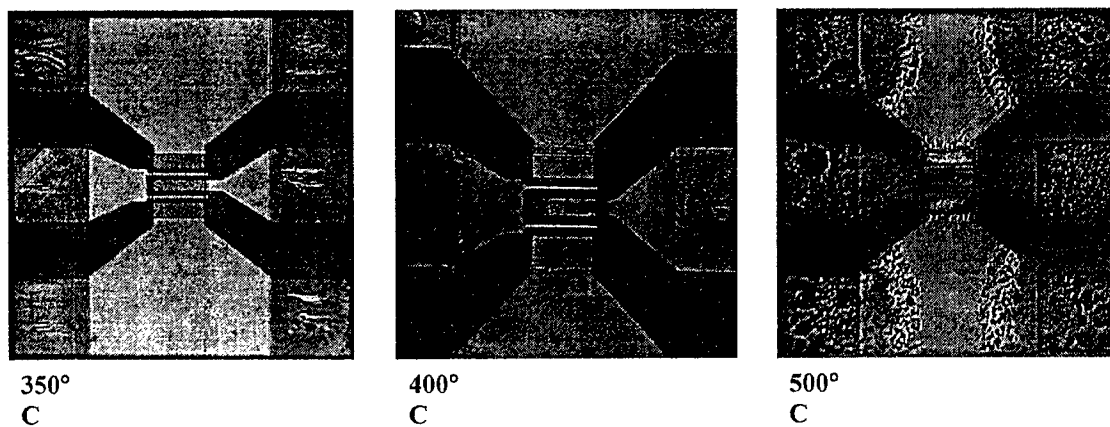


Figure 4.2.1. Images of HEMT device post in-situ thermal annealing/cleaning.

In collaboration with Bob Fitch at WPAFB, we have conducted a preliminary study employing iridium in the metal contact scheme. The enhanced thermal stability of this metal scheme has allowed for in-situ thermal cleaning temperatures to be increased up to 650°C, allowing for a much cleaner nitride surface ready for passivation. As seen in Figures 4.2.2 and 4.2.3, these devices showed significant improvement over similar devices annealed only to 300°C prior to oxide deposition, as evidenced by a 20% increase in I_{ds} for the 650°C anneal compared to 6-10% increase in I_{ds} for the 300°C annealed

HEMT device. Both devices were passivated with Sc_2O_3 . Gain and P_{out} were also increased relative to the 300°C annealed/passivated HEMT. Feasibility of using this or similar metal schemes are under investigation.

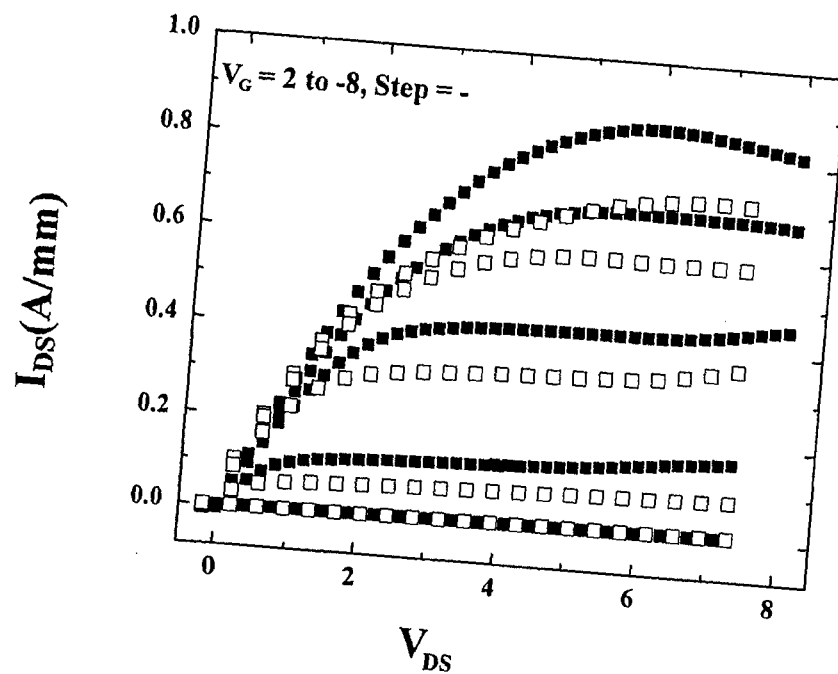


Figure 4.2.2. V_{DS} - I_{DS} of HEMT device with Ir gate metal scheme after thermal cleaning at 650°C.

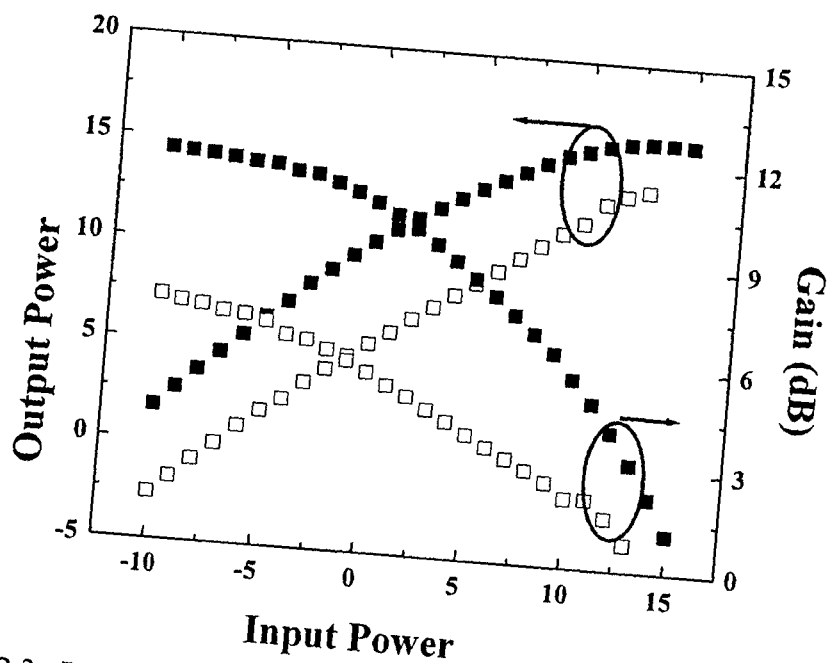


Figure 4.2.3. Power Performance of HEMT device with Ir gate metal scheme after thermal cleaning at 650°C.

4.2.2 Passivation treatment effects on source and drain contact resistance

Since the in-vacuum anneal has been shown to be a key component in reducing the current collapse of the HEMT devices, its effect on the other components of the device, namely the contacts, must be studied. Typical Ohmic contacts (Ti/Al/Pt/Au) were deposited by electron beam evaporation onto GaN substrates. A control sample was annealed in an AG Associates 610 RTA in flowing nitrogen at 750°C for 1 minute. All other vacuum anneals and treatments were compared to this control sample to determine the effectiveness. The in-vacuum annealing conditions were 700°C for 5 minutes at a background pressure of 1×10^{-9} Torr. Prior to the in-vacuum anneal, samples were subjected to either UV-ozone or buffered oxide etch solution of (6:1) ammonium fluoride:hydrofluoric acid (BOE). The BOE treatment is indicated as pretreatment for further reference. The current-voltage results of these treatments and the subsequent vacuum anneals are plotted in figure 4.2.4.

The comparison of these treatments and anneals indicates that neither the pretreatment, or the UV-ozone, and the in-vacuum anneals adversely effected the contact resistance. In fact, the contact resistance after the treatments and in-vacuums anneals is lower than the conventional RTA anneals. Therefore the pretreatments and in-vacuum anneal are fully compatible with source and drain metal contact stacks currently used to fabricate AlGaIn/GaN HEMT devices.

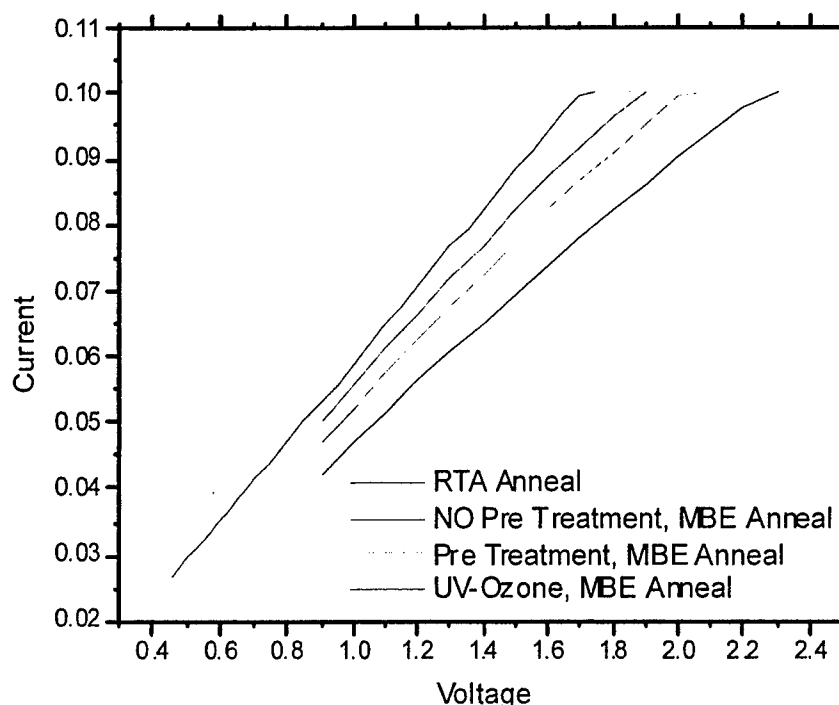


Figure 4.2.4 Current-Voltage results of treatments and vacuum anneals compared to a conventional RTA anneal.

A further study of gate metal will be conducted to determine the passivation treatment effects on the Schottky. We have learned that the final metal layer becomes easily damaged from the in-vacuum anneal as low as 400°C. To date, this is the limiting factor for the high temperature annealing. A change in processing sequence that provides

the passivation layer earlier in the fabrication process can eliminate the need for a high temperature anneal post final metallization. This is currently the process sequence that several of the HEMT groups are employing and are finding success.

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4.3 Task 3: Optimized Dielectric Deposition

4.3.1 Upgrade of oxide GSMBE system to 2" or 3" wafer capability

One of the major objectives of the first year of the program was to upgrade the oxide MBE system from a maximum substrate size of 2" diameter (usable area typically only 1.5" diameter) to 3" diameter. This required a complete redesign of the source shroud and source flange. In addition, the substrate heater and sample transfer mechanism was converted from the Riber style to the Varian style so that transfer between the oxide system, the nitride MBE system and the UHV STM/AFM system can be accomplished without exposing samples to air. As shown in Figures 4.3.1 and 4.3.2, this upgrade has improved the thickness uniformity from 22% center to edge to 12% center to edge. Further improvements in uniformity would require upgrading of the effusion cells. The present configuration, however, appears to be adequate for uniform passivation of GaN HEMTS.

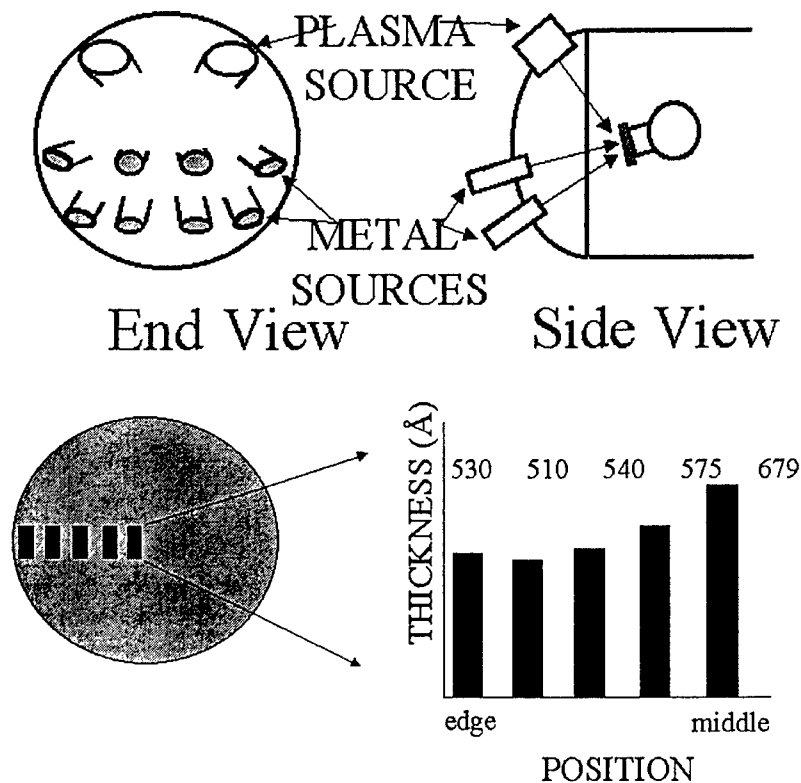


Figure 4.3.1. Original configuration of oxide MBE source flange (at top) and thickness uniformity across 2" wafer (bottom). Note that the oxygen plasma source was not in an "optimum" position for uniformity, resulting in an MgO thickness variation of ~22% from center to edge.

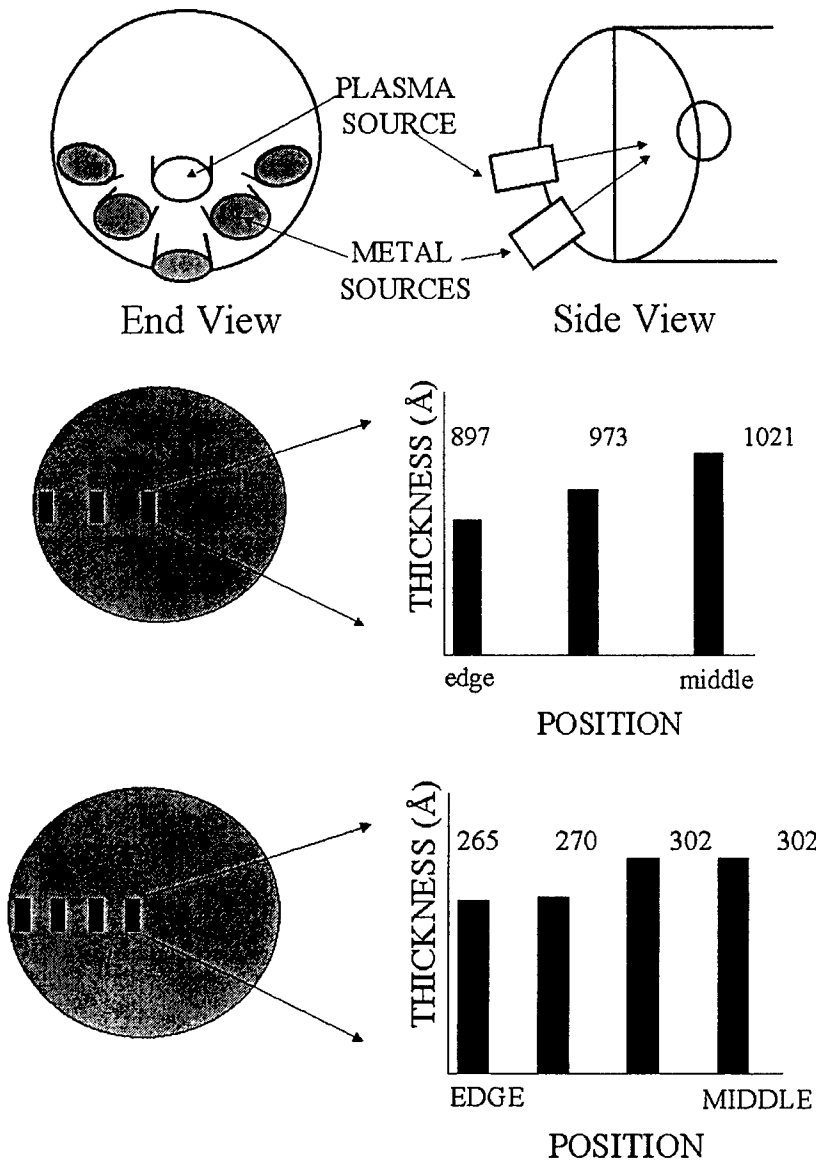


Figure 4.3.2. New source flange configuration for oxide MBE system used for passivation (at top). Thickness uniformity across a 2inch wafer for MgO (middle) and Sc₂O₃ (bottom). Variation in both cases is ~12% from center to edge.

4.3.2 Determination and optimization of dielectric microstructure

From examining the cross-section TEM images of (111) MgO on (0001) GaN and (111) Sc₂O₃ on GaN, shown in Figure 4.3.3, it has been determined that the first few monolayers of MgO or Sc₂O₃ deposited are single crystal, even at growth temperatures as low as 100°C. It is assumed that these single crystal, epitaxial layers minimize the density of dangling bonds at the interface and are thus responsible for the low interface state densities observed in our oxide/GaN structures. The fact that the layers are epitaxial underscores the need for obtaining a clean GaN surface prior to deposition. While the low 100°C growth temperature is desirable from the standpoint of minimizing the HEMT thermal exposure, it does complicate the cleaning of the GaN or AlGaN starting surface.

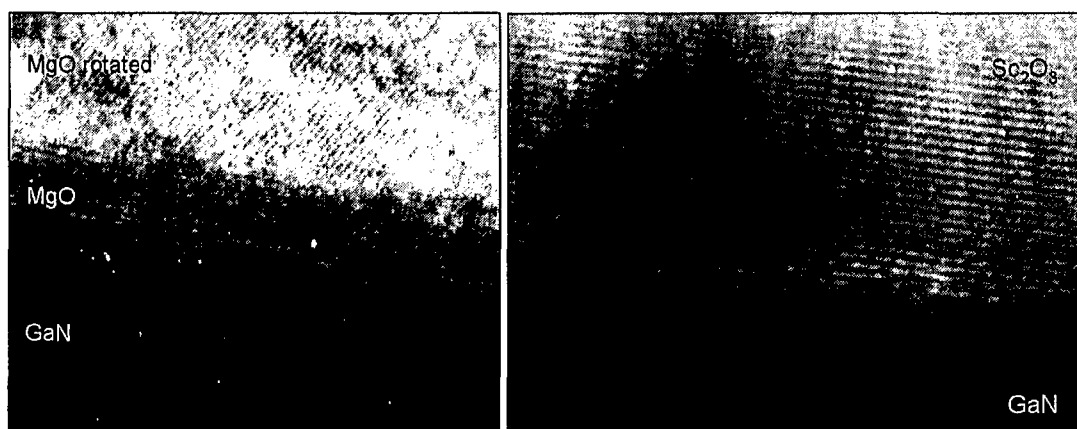


Figure 4.3.3. XTEM images of MgO/GaN (at left) and Sc₂O₃/GaN (at right) showing the single crystal, epitaxial nature of the initial oxide growth.

Prior to funding of this program we had developed a passivation recipe which was found to work well with GaN capped structures. Optimized HEMT devices however are now employing AlGaIn capped structures and initial work showed our previous recipe to be inadequate for structures with ~25% Al in the cap layer. To refine the passivation recipe employed for these types of structures, experiments were performed to optimize the oxygen plasma conditions used for deposition of the Sc₂O₃ passivation. The HEMT material for this study was provided by Bob Fitch (WPAFB). Plasma power was varied from 250 Watts to 350 Watts. As shown in Table I, it was found that 325 Watts forward power gave an optimum passivation. Changing the oxygen pressure was found to further improve the passivation, with a final pressure of 8×10^{-6} Torr providing the best performance.

Table I. Dependence of passivation on plasma power and oxygen pressure.

Plasma Forward Power (Watts)	Oxygen Pressure (Torr)	Passivation (%)
250	8×10^{-6}	4.5
275	8×10^{-6}	4.9
325	8×10^{-6}	83.6
325	10×10^{-6}	67.9
350	8×10^{-6}	3.0

4.3.3 Device Improvement through the use of Sc₂O₃ For Both Passivation and Gate Dielectric

Though we have previously demonstrated that MgO can provide significant improvement in device performance when used as a passivating dielectric, development of environmentally stable MgO-based films is still in progress. In the interim, we have explored Sc₂O₃ as an environmentally stable alternative. Sc₂O₃ exists in the Bixbyite structure, has a bandgap of 6.3eV and dielectric constant of 14. In spite of the large

lattice mismatch to GaN, 9.2%, the presence of a single crystal oxide at the oxide/semiconductor interface has been indicated by in-situ RHEED analysis, ex-situ XRD and XTEM as shown previously in this section.

HEMT layer structures were grown on C-plane Al_2O_3 substrates by Metal Organic Chemical Vapor Deposition (MOCVD) in a rotating disk reactor. The layer structure included an initial $2\mu\text{m}$ thick undoped GaN buffer followed by a 35nm thick unintentionally doped $\text{Al}_{0.28}\text{Ga}_{0.72}\text{N}$ layer. The sheet carrier concentration was $\sim 1 \times 10^{13} \text{cm}^{-2}$ with a mobility of $980 \text{cm}^2/\text{V-s}$ at room temperature. Mesa isolation was formed by Cl_2/Ar Inductively Coupled Plasma etching at 5mTorr pressure, 300W of 2MHz source power and 40W of rf chuck power so that the average ion energy was $\sim 90\text{eV}$. The source/drain ohmic contacts was formed by lift-off of e-beam deposited $\text{Ti}(200\text{\AA})/\text{Al}(1000\text{\AA})/\text{Pt}(400\text{\AA})/\text{Au}(800\text{\AA})$. The contacts were annealed at 850°C for 45sec under a flowing N_2 ambient in a Heatpulse 610T system. Two different types of experiments were performed. In the first, one of the wafers was divided in half and on one piece 400\AA Sc_2O_3 was deposited as a gate dielectric. Before oxide deposition, the wafer was exposed to ozone for 25 minutes. It was then rinsed in a 1:1 ratio of BOE: H_2O treatment for 1min followed by in-situ 650°C cleaning for 10mins inside the growth chamber. The Sc_2O_3 was deposited by rf plasma-activated MBE at 100°C using elemental Sc evaporated from a standard effusion all at 1130°C and O_2 derived from an Oxford RF plasma source. The plasma conditions were the same as outlined in the previous section. Final metal of e-beam deposited Pt/Au ($1 \times 60 \mu\text{m}^2$) gate contacts was employed on both the HEMTs and MOS-HEMTs. The purpose of this experiment was to compare the performance of the conventional metal-gate HEMTs with the Sc_2O_3 MOS-HEMTs.

In the second experiment, another wafer was fabricated as conventional metal-gate HEMTs by the same process as described above. Half of the samples, Sc_2O_3 was deposited as a surface passivation layer at 100°C . In this case, the pre- Sc_2O_3 -deposition treatment consisted of ozone exposure for 25 min. followed by an in-situ thermal treatment at 300°C . The purpose of this experiment was to examine the effectiveness of the Sc_2O_3 as a passivation layer.

The dc characteristics of all of the devices from room temperature measurements were measured on an Agilent 4156C parameter analyzer. The on-wafer power measurements were performed on a load-pull system using mechanical tuners for network matching and there was no harmonic termination under class A operation. The passivated devices were matched for the power testing prior to passivation and were tested under these same conditions after Sc_2O_3 deposition.

MOS-HEMT versus HEMT devices

Figure 4.3.4 shows the transfer characteristics for both HEMTs and Sc_2O_3 MOS-HEMTs. The threshold voltage of the MOS-HEMTs shifted to more negative values relative to the HEMTs because of the longer gate-to-channel separation with additional Sc_2O_3 under the gate contact. Note that the drain current is increased from $\sim 0.6\text{A/mm}$ to $\sim 0.75\text{A/mm}$. The threshold voltages for the two types of devices was in good agreement with the values expected from the equation $\frac{en_s}{C_b}$, where e is the electronic charge, n_s the

sheet carrier density and C_b the total capacitance per unit area of the barrier layer and Sc_2O_3 .

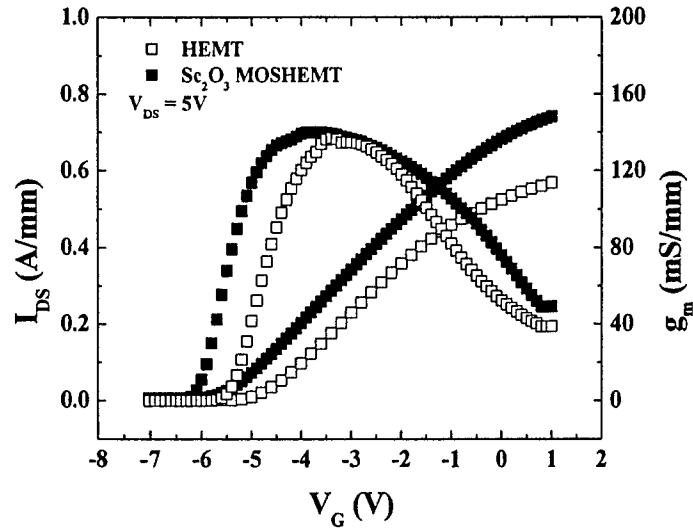


Figure 4.3.4. Transfer characteristics for MOS-HEMTs and HEMTs fabricated on the same wafer. The drain-source voltage was 5V.

The drain I-V characteristics of devices are shown in Figure 4.3.5. The MOS-HEMTs show a slightly better knee voltage and higher output conductance. The MOS-HEMT clearly showed much better gate modulation to +2V as compared to that of conventional Schottky gate on the conventional HEMTs.

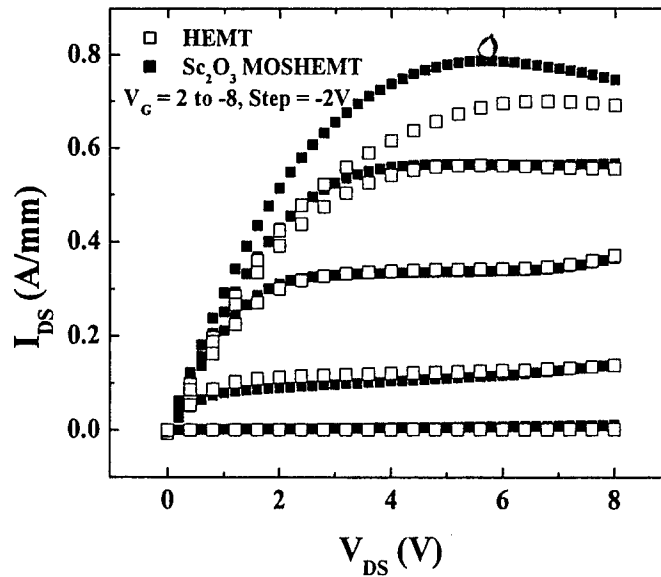


Figure 4.3.5. I_{DS} - V_{DS} characteristics for $1 \times 60 \mu\text{m}^2$ MOS-HEMTs and HEMTs fabricated on the same wafer. The gate voltage was varied from 2 to -8V in steps of -2V.

Figure 4.3.6 shows typical load-pull data for the two types of devices at a measurement frequency of 4GHz in both cases. The drain voltage was held at 10V with a gate voltage of -3V. The MOS-HEMT has higher output power and associated gain over the entire input power range investigated. The power-added efficiency, as illustrated in

Figure 4.3.7, was also significantly improved ($\sim 27\%$) relative to the HEMT ($\sim 5\%$). In the latter case the unpassivated surface leads to severe reductions in output power and power-added efficiency due to the current collapse problem.

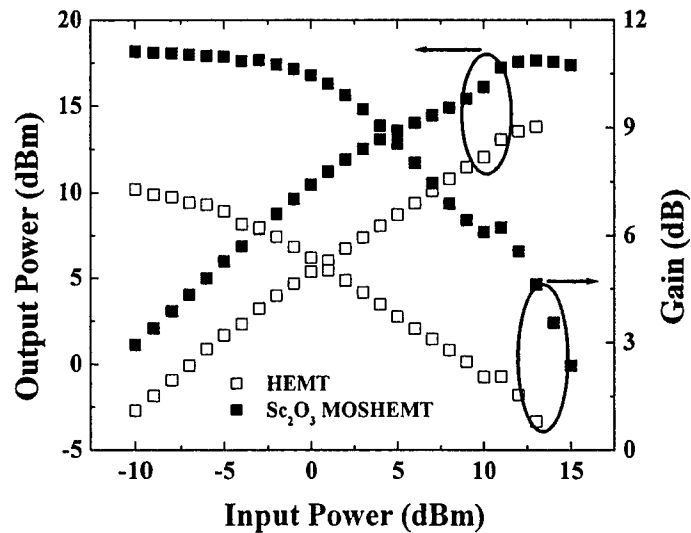


Figure 4.3.6. Output power and gain vs input power at 4GHz of $1 \times 60 \mu\text{m}^2$ MOS-HEMTs and HEMTs fabricated on the same wafer.

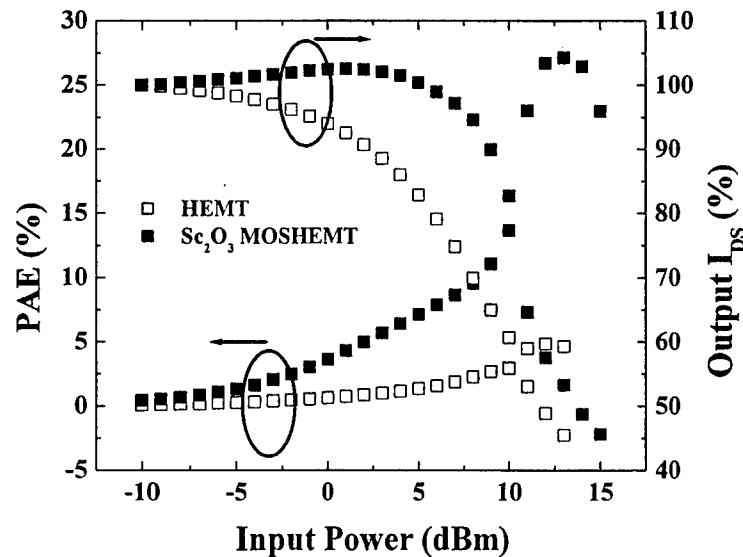


Figure 4.3.7. Power-added efficiency at 4GHz of $1 \times 60 \mu\text{m}^2$ MOS-HEMT and HEMTs fabricated on the same wafer.

Sc₂O₃ Passivation

Even without a MOS-gate, the HEMT performance is significantly improved by the presence of the Sc_2O_3 surface passivation layer. Figure 4.3.8 shows the output curves of metal-gate HEMTs with and without Sc_2O_3 passivation. Once again the drain current improves due to a reduction in the carrier depletion effects of the surface. Similar conclusions are drawn from the transfer characteristics in Figure 4.3.9. The saturation drain-source current increases from 0.55A/mm to 0.75A/mm with deposition of the Sc_2O_3 .

passivation layer and the threshold voltage shifts to more negative values because of the increase in effective channel carrier density.

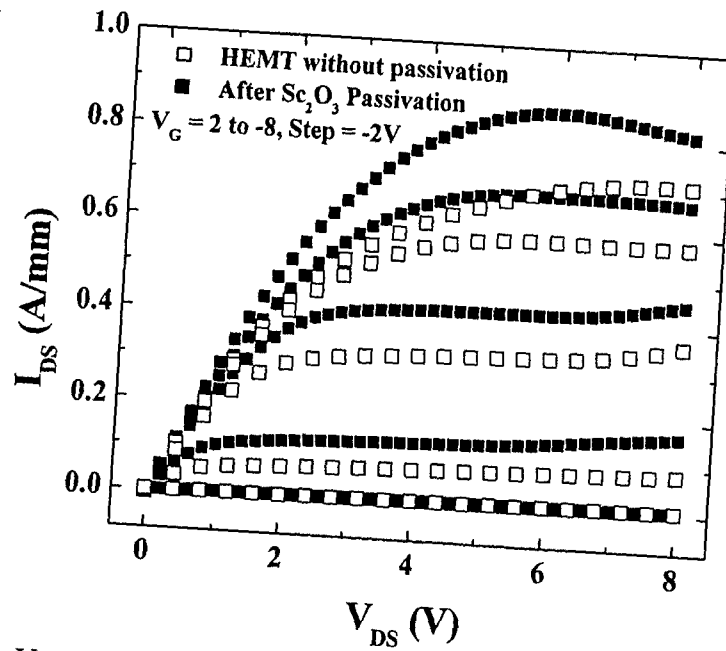


Figure 4.3.8. I_{DS} - V_{DS} characteristics for $1 \times 60 \mu m^2$ HEMTs with and without Sc_2O_3 passivation. The gate voltage was varied from 2 to -8V in steps of -2V.

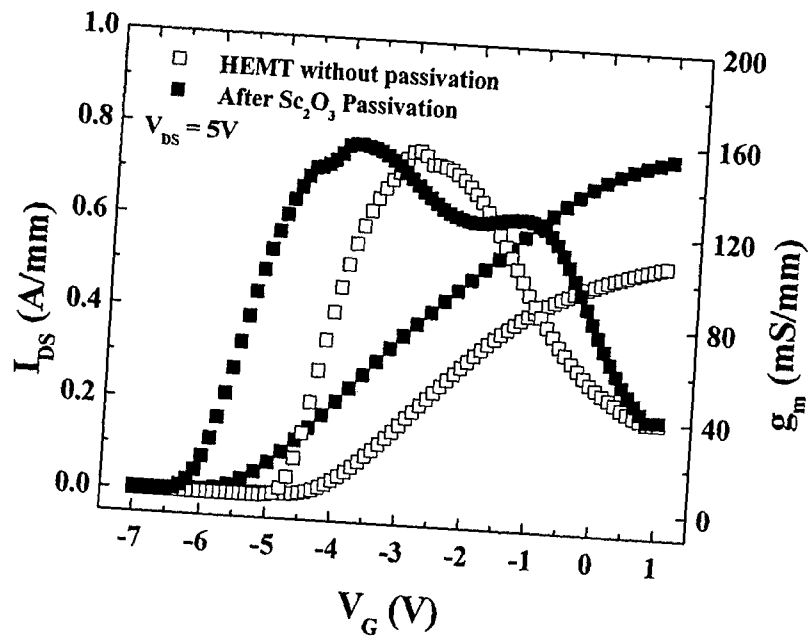


Figure 4.3.9. Transfer characteristics for $1 \times 60 \mu m^2$ HEMTs with and without Sc_2O_3 passivation. The drain voltage was -5V.

The reduction in forward and reverse leakage was quite evident on the passivated HEMTs, as shown in Figure 4.3.10. This is consistent with a reduction in surface

recombination center density and the series resistance of the HEMT is reduced due to the reduction in surface depletion effects on the channel carrier density. This same effect leads to an increase in reverse breakdown voltage.

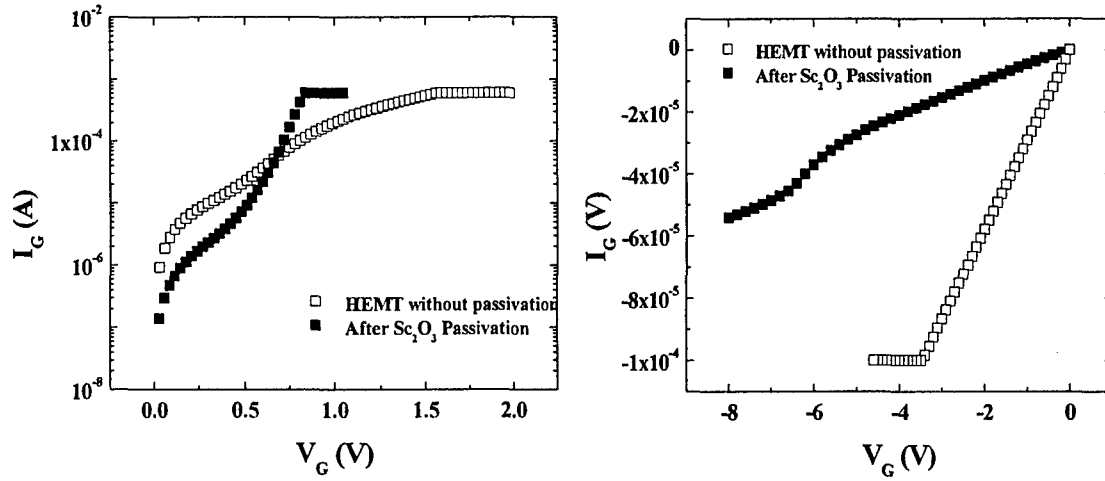


Figure 4.3.10. Forward (at left) and reverse (at right) I-V characteristics from $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation.

In addition, we observed an increase in the three-terminal breakdown voltage as seen in the $I_{\text{DS}}-V_{\text{DS}}$ curves at -9 V of gate bias voltage of Figure 4.3.11. In this measurement, a gate voltage of -8 V was applied to fully deplete the channel and the I_{DS} remaining is the leakage current that cannot be modulated by the gate. Defining breakdown as the voltage at which the current density is 1 mA/mm , the addition of the Sc_2O_3 layer increases the three-terminal breakdown voltage from 11 to 15 V . This is important especially for output power of the HEMT because unmodulated leakage current will decrease power-added efficiency (PAE) at high drive conditions and an increase in 3 terminal breakdown voltage increases the range of V_{DS} that can be used. The gate reverse leakage current was also significantly decreased after Sc_2O_3 passivation. This is the first report of an increase in three-terminal drain breakdown voltage of an AlGaIn/GaN HEMT after any form of surface passivation.

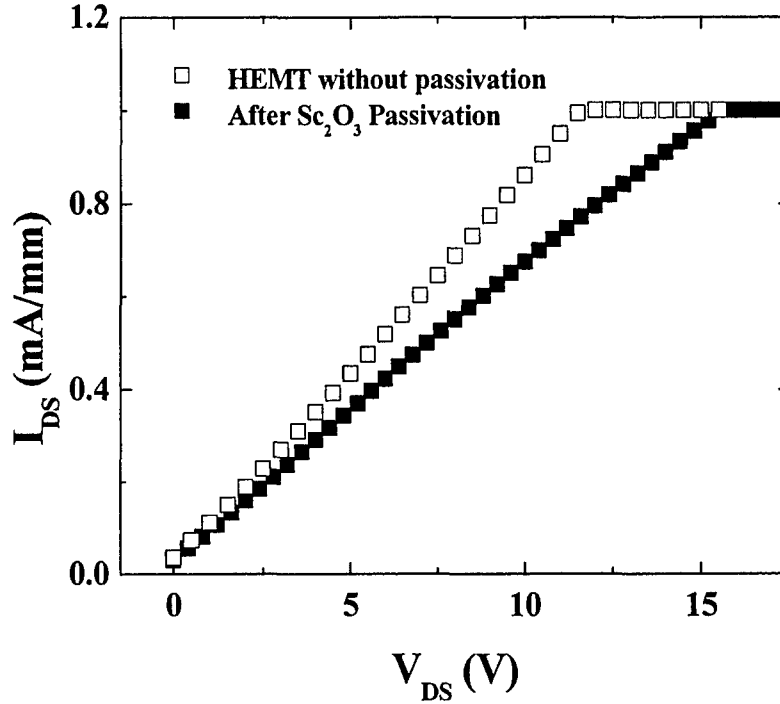


Figure 4.3.11. Forward I_{DS} - V_{DS} characteristics from $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation.

The output power characteristics of the Sc_2O_3 -passivated HEMTs were significantly better than those of the comparison, unpassivated devices from the same wafer. Figure 4.3.12 shows the power sweep curves at 4GHz under class A conditions for passivated and unpassivated HEMTs. The on-wafer measurements were performed on a load-pull system using mechanical tuners for matching and there was no harmonic termination. The unpassivated devices were enabled for the power testing prior to passivation and were tested under these same conditions after Sc_2O_3 deposition. The effect of the passivation is to increase the output power by approximately a factor of four over the range -10 to 7dBm and there is still a factor of approximately two increase at the highest input power. This is a clear demonstration of the ability of Sc_2O_3 layers to suppress the effects of surface-related deep trap states which otherwise lead to depletion of the channel and large signal gain collapse. The power-added efficiency also shows a major improvement from ~5% to 12% as a result of the passivation (Figure 4.3.13). The low PAE of the unpassivated HEMT is most likely due to the presence of surface states that decrease the output current. The PAE is calculated from the equation:

$$\text{PAE} = (P_{\text{out_delivered}} - P_{\text{in_delivered}}) / (\text{DC Power})$$

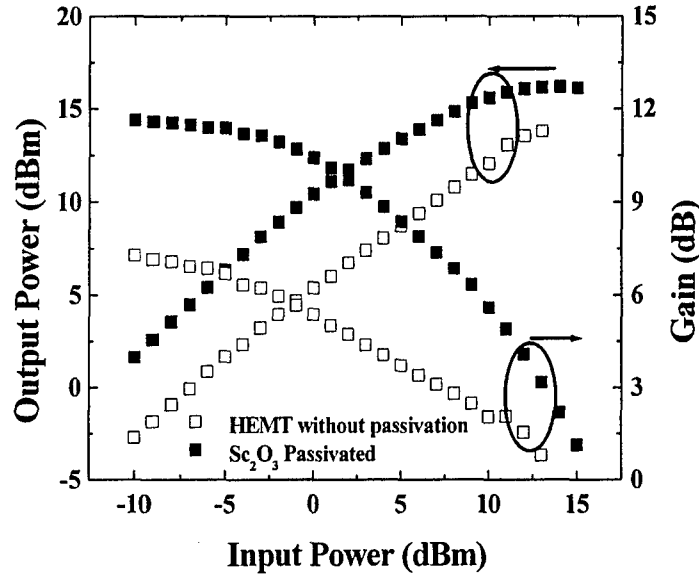


Figure 4.3.12. Output power and gain vs input power at 4GHz of $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation.

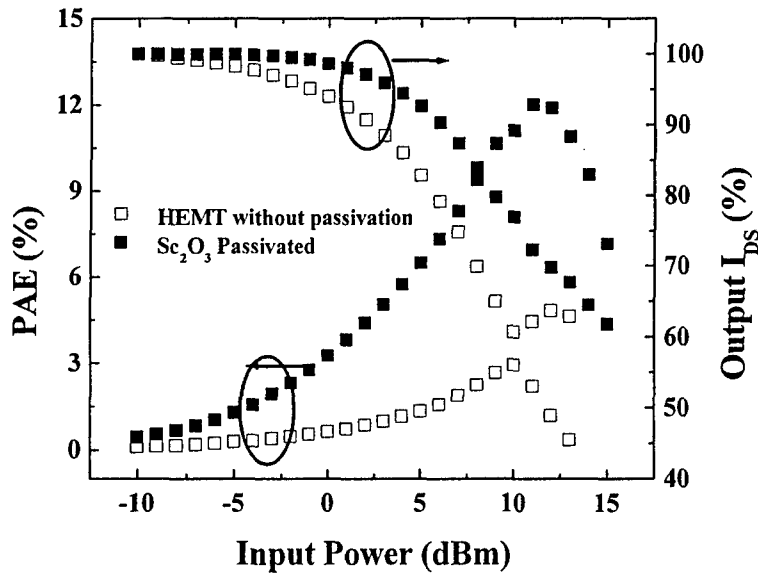


Figure 4.3.13. Power-added efficiency at 4GHz of $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation.

In the case of the MOS-HEMT, PAE is high because the output power remains high even as output current decreases. Figure 4.3.14 shows $I_{\text{DS}}-V_{\text{DS}}$ sweep characteristics for an unpassivated HEMT. There is an obvious decrease in the I_{DS} around the knee voltage as the measurements are repeated. This phenomenon was not observed on the passivated HEMTs or on the MOS-HEMTs and suggests the low PAE of the unpassivated device is due to the presence of surface states. A summary of the PAE data is shown in Table II.

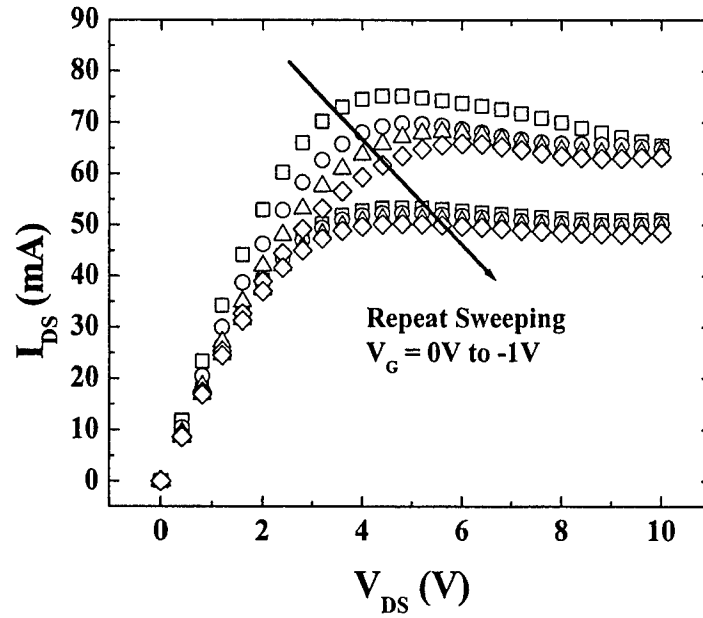


Figure 4.3.14. I_{DS} - I_{DS} sweep measurements of unpassivated HEMT. The V_{DS} is swept from 0V to 10V, with $V_G = 0V$ to $-1V$ in $-1V$ step. This phenomenon is not observed on passivated HEMTs or on MOS-HEMTs.

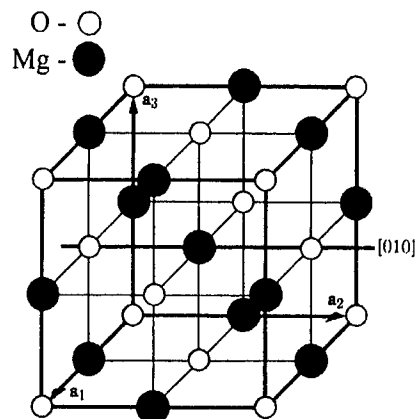
Table II. Power-added efficiency of unpassivated, Sc_2O_3 passivated and Sc_2O_3 MOS-HEMT as a function of V_{DS} .

V_{DS} Bias Voltage	Power-added Efficiency (PAE)		
	Unpassivated HEMT	Sc_2O_3 Passivated HEMT	Sc_2O_3 MOS-HEMT
5V	3.5%	6.4%	24.5%
10V	4.8%	12%	27.1%
15V	3.6%	13.2%	18.6%

4.3.4 Growth of CaO

It is expected that by lattice matching the oxide to the GaN, the interfacial trap density can be reduced. One method of accomplishing this is to alloy the MgO with an oxide of larger lattice constant. Calcium oxide was chosen for this purpose because CaO is also a rock salt dielectric, Figure 4.3.15, like MgO, but has a larger lattice constant, 4.779Å. The CaO dielectric constant (11.8) and bandgap (7.1eV) are similar to those of MgO. From Vegard's Law, the optimum ratio of Mg:Ca should be 1:1 in order to get material lattice matched to GaN. Though the phase diagram shows poor miscibility between MgO and CaO, single-phase thin films on GaAs whose compositions span the entire composition range have been reported using LT-MBE as the deposition method².

Figure 4.3.15 Illustration of the rock salt structure (from Cullity 1978).



Starting with conditions similar to those used for the growth of MgO, CaO films were grown on GaN. The solid metal Ca source was set at a temperature of 405°C to achieve a flux of 8×10^{-8} Torr as was the same flux used for the growth of MgO. The RF oxygen plasma was set at a pressure of 2×10^{-5} Torr and the substrate temperature was 100°C or 300°C. AES showed evidence of CaO deposition, Figure 4.3.16, but XRD showed no additional CaO or Ca peaks. TEM confirmed that the film was polycrystalline at the interface but amorphous after 2.0nm, Figure 4.3.17. The amorphous nature of the bulk of the film explains the absence of peaks in XRD. The growth rate of CaO at 100°C was 2.6 nm/min, while at 300°C the growth rate was 2.2 nm/min. This is to be expected since an increase in temperature should decrease the sticking coefficient. AFM shows no change in RMS roughness in CaO grown at 100°C or 300°C but stays constant at about 0.667 nm, Figure 4.3.18.

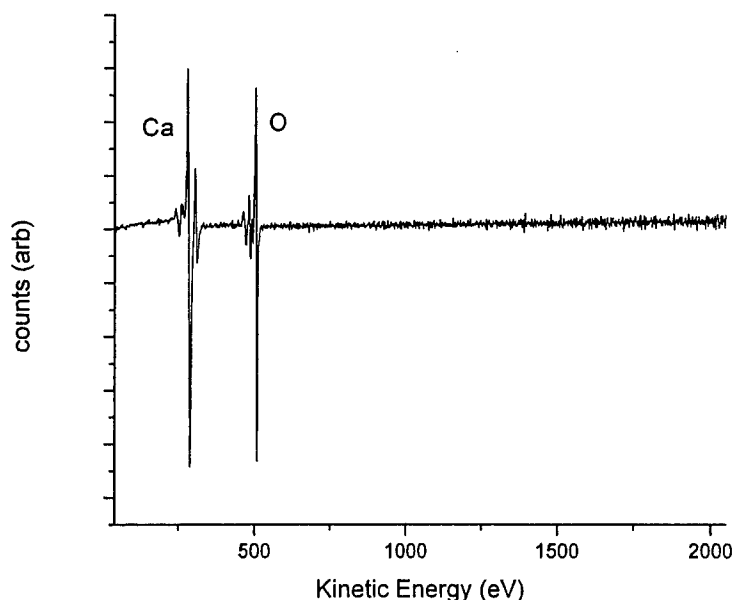


Figure 4.3.16 AES shows only Ca and O after growth of CaO at 300°C

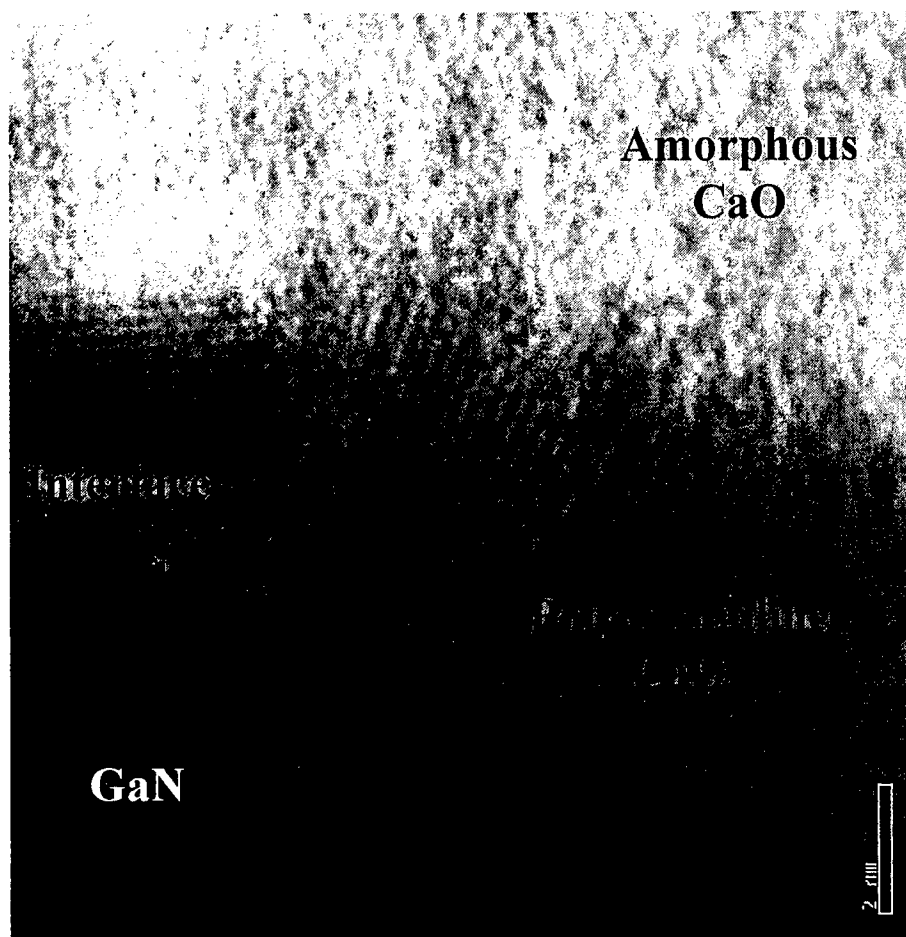


Figure 4.3.17 HR TEM of CaO.

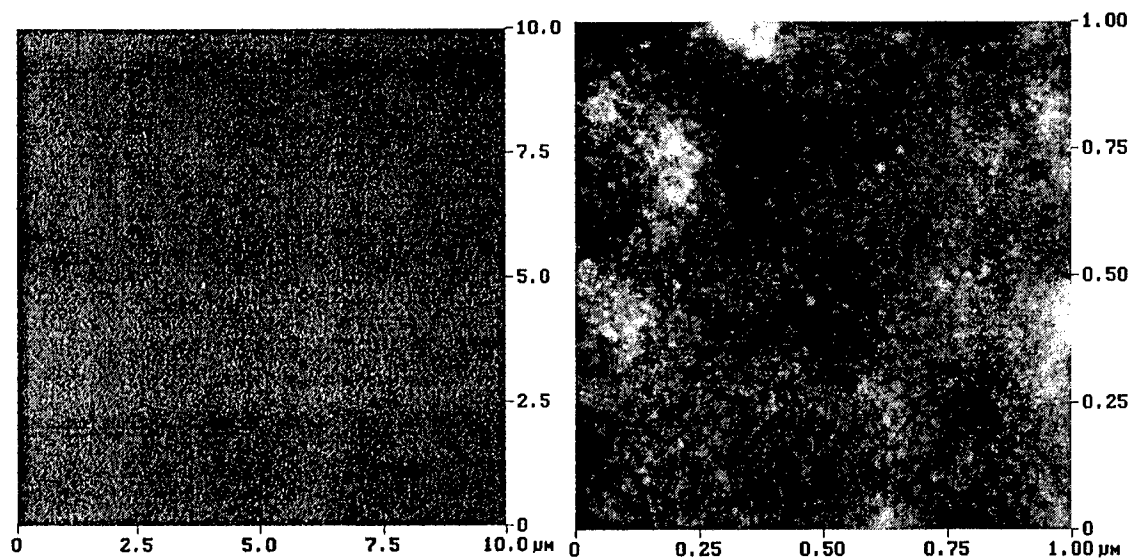


Figure 4.3.18. AFM of CaO grown at 100°C, at left, and 300°C, at right.

4.3.5 Growth of Ternary MgCaO

The standard MgO growth conditions have produced oxide/GaN interfaces with low D_{it} consist of a Mg beam equivalent pressure, BEP, of 10×10^{-8} Torr. The addition of Ca to this beam at a comparable Ca BEP of 8×10^{-8} Torr, produced an increase of less than 50% in growth rate. This suggests that the sticking coefficient of the Ca is significantly lower than that of the Mg. This is further confirmed by AES analysis, which shows a Mg/Ca ratio less than that expected for a 50/50 composition film, Table III. In addition, AES depth profiling analysis shows that the Ca has severely segregated to the surface, Figure 4.3.19. This would also indicate a low Ca sticking coefficient.

Table III: Growth rate and AES data for MgCaO samples. AES data taken from an MgO single crystal is shown for comparison.

Mg Beam Equivalent Pressure (Torr)	Ca Beam Equivalent Pressure (Torr)	Growth Rate (nm/min)	Mg/Ca Ratio	(Mg+Ca)/O Ratio
5.7×10^{-8}	5.7×10^{-8}	1.0	0.81	0.92
10×10^{-8}	8×10^{-8}	5.3	1.27	0.83
10×10^{-8}	-	3.4	0.72	0.72
MgO Ref.	-	-	-	0.6

In spite of the apparent segregation of the Ca, XRD analysis of the MgCaO layer shows no evidence of phase separation, Figure 4.3.20. MgO layers grown under similar conditions typically show primarily a (222) peak due to the texturing of the film. The MgCaO layer shows no evidence of either the MgO or the CaO (222) peaks suggesting that phase separation into the two binaries has not occurred. Instead there appears to be a shoulder on the GaN (004) peak that is not observed in spectra taken from either GaN substrates or MgO layers grown on GaN. This peak is most likely the (222) peak from the ternary MgCaO. The peak position is shifted to larger plane spacing relative to the MgO peak as would be expected from the addition of Ca, Figure 4.3.21. The proximity of this peak to the GaN (004) peak is encouraging and suggests that the addition of Ca may be useful in reducing the lattice mismatch between the dielectric and the GaN. Unfortunately due to the severe segregation, the peak is broadened indicative of a range of compositions present in the film, Figure 4.3.22.

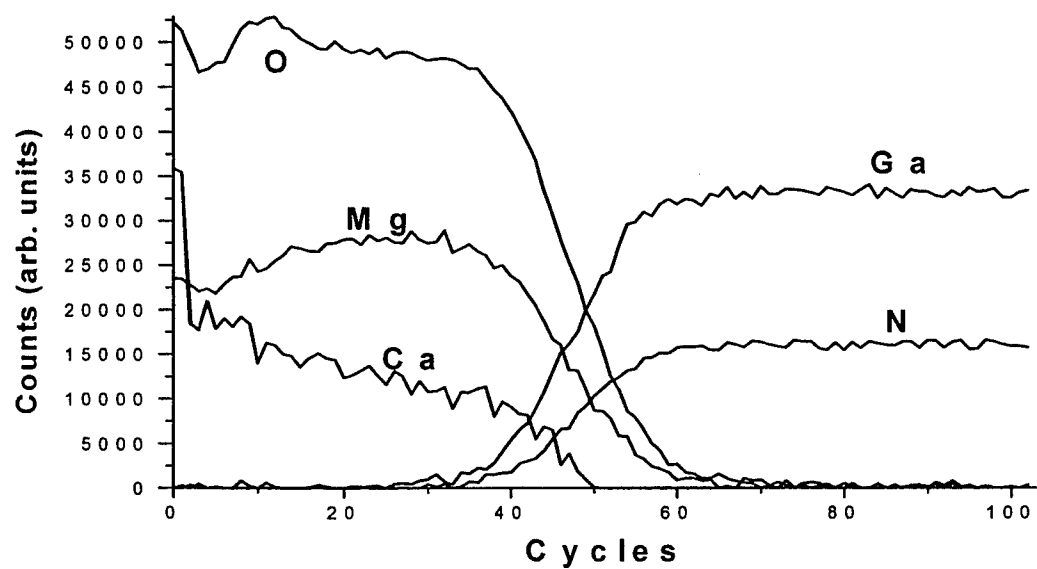
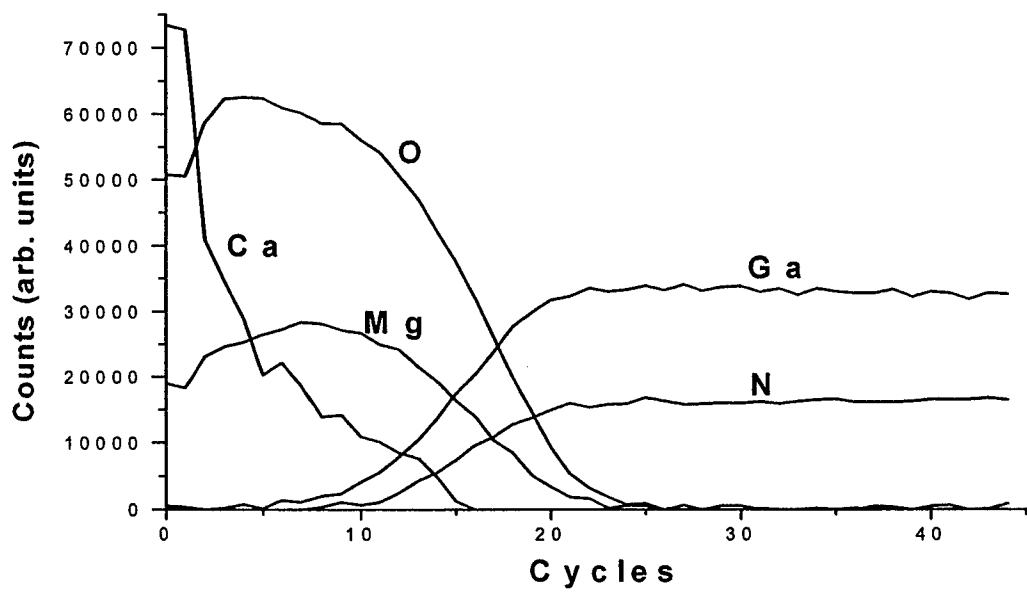


Figure 4.3.19. AES depth profiling of MgCaO grown using Ca and Mg BEP of 5.7×10^{-8} and 5.7×10^{-8} (top) and 8×10^{-8} and 10×10^{-8} (bottom).

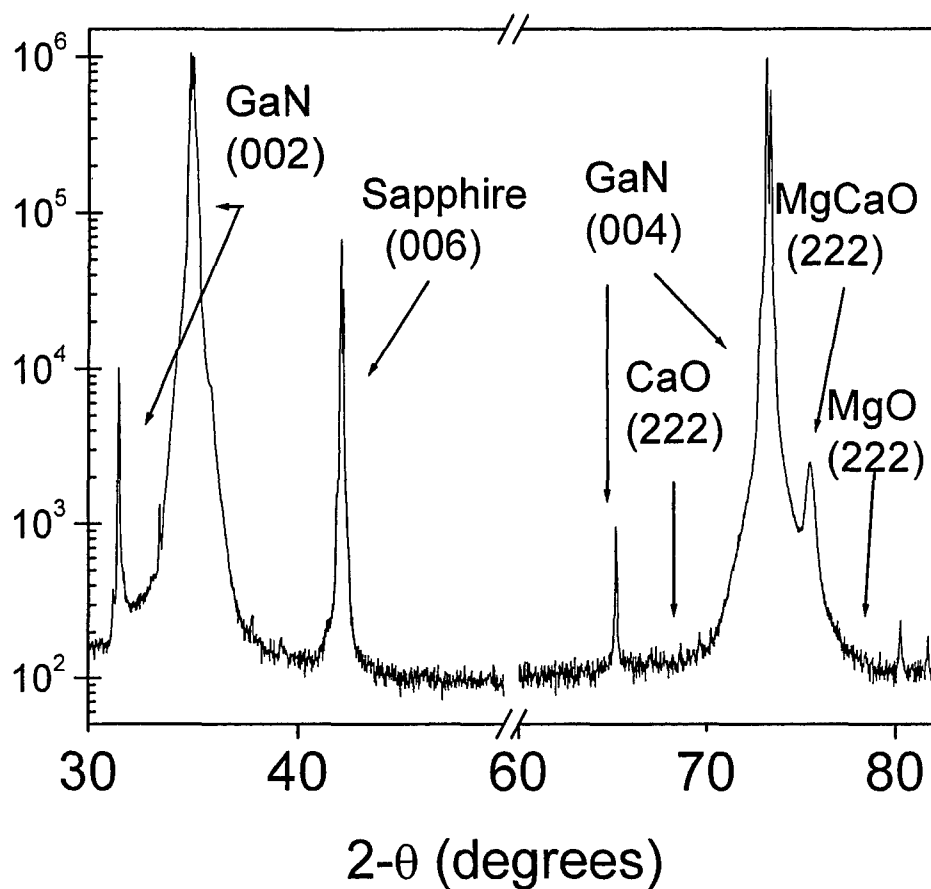


Figure 4.3.20. XRD of MgCaO shows no signs of phase separation or secondary phases.

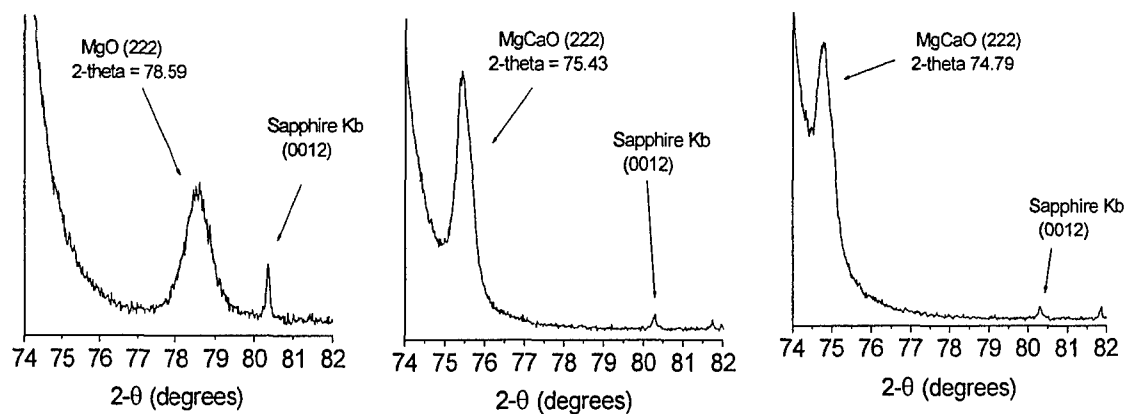


Figure 4.3.21. Powder XRD showing increase in lattice constant with the addition of increasing amounts of Ca.

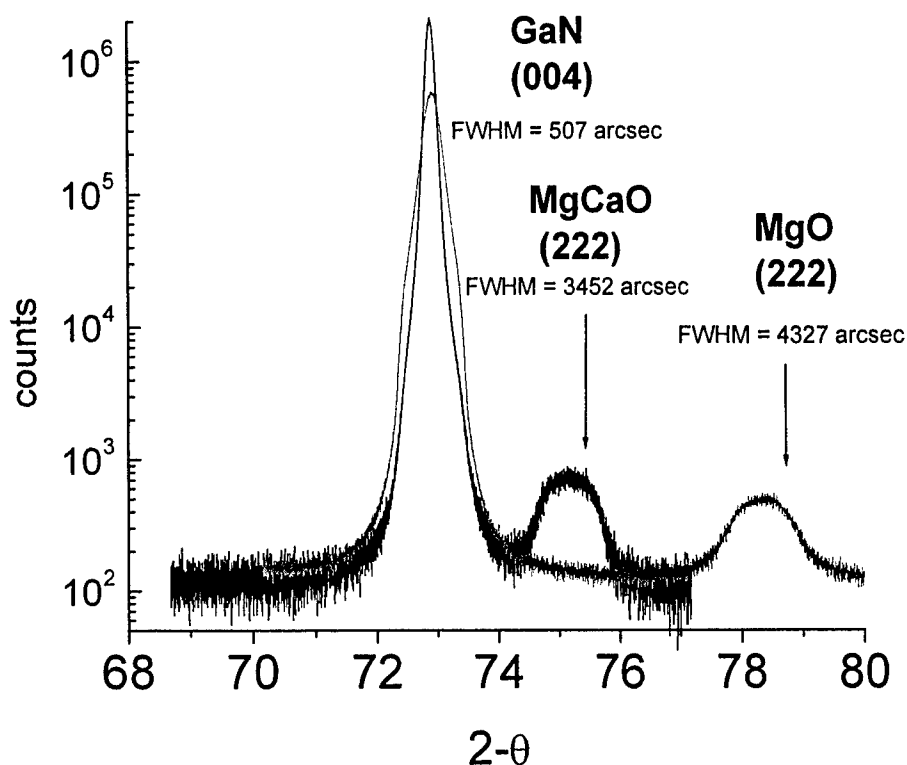


Figure 4.3.22. HR-XRD shows the relative positions of the MgO (222) and the MgCaO (222) peaks.

AFM analysis of the ternary grown at the highest flux rates shows a very rough surface morphology, Figure 4.3.23. MgO layers grown under similar conditions show smooth morphology with an RMS of $\sim 1\text{nm}$, suggesting that the Ca addition has dramatically altered the microstructure. It was thought that the higher growth rate used for the deposition of the ternary might have caused the rough morphology. To investigate a lower growth rate, the fluxes were reduced to $\text{BEP} \sim 5.7 \times 10^{-8} \text{ Torr}$. This did produce a substantial drop in the growth rate to $\sim 1 \text{ nm/min}$ and was successful in improving the surface morphology. Reducing the growth rate did not, however, suppress the Ca segregation in fact there appears to be even greater disparity in the Ca surface and interface concentrations. This is not surprising since lower growth rates are usually found to enhance segregation.

Substrate temperature also affects the growth of MgCaO. At a substrate temperature of 340°C , no film was grown even after 20 minute of growth time as determined by AES. AES from a film produced at a slightly lower substrate temperature of 300°C showed that a film was present, Figure 4.3.24. This film has a reasonable growth rate of 5.2 nm/min , and enhanced crystallinity as shown by XRD, Figure 4.3.25. For this substrate temperature, AFM does show a slightly rougher surface than that produced with a substrate temperature of 100°C , Figure 4.3.26. Due to improvements in film quality with the increased substrate temperature, all further growths were done at a substrate temperature of 300°C .

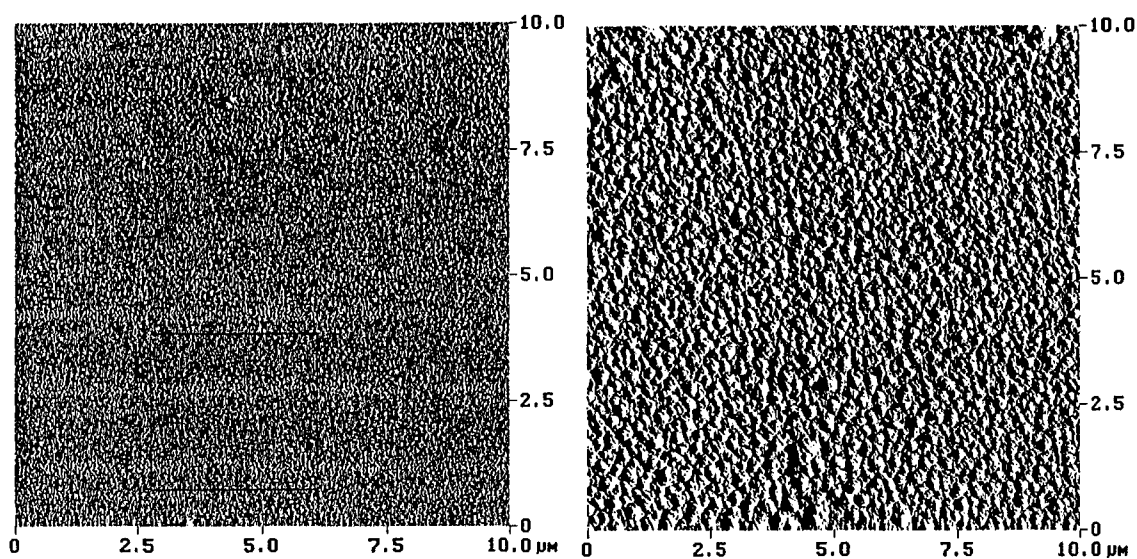


Figure 4.3.23. AFM of MgCaO grown at 100°C using Mg and Ca fluxes of 5.7×10^{-8} (at left) or 8×10^{-8} (at right). RMS roughnesses for the two samples were 4nm and 9nm respectively. MgO grown under similar conditions shows an RMS roughness of ~ 1 nm

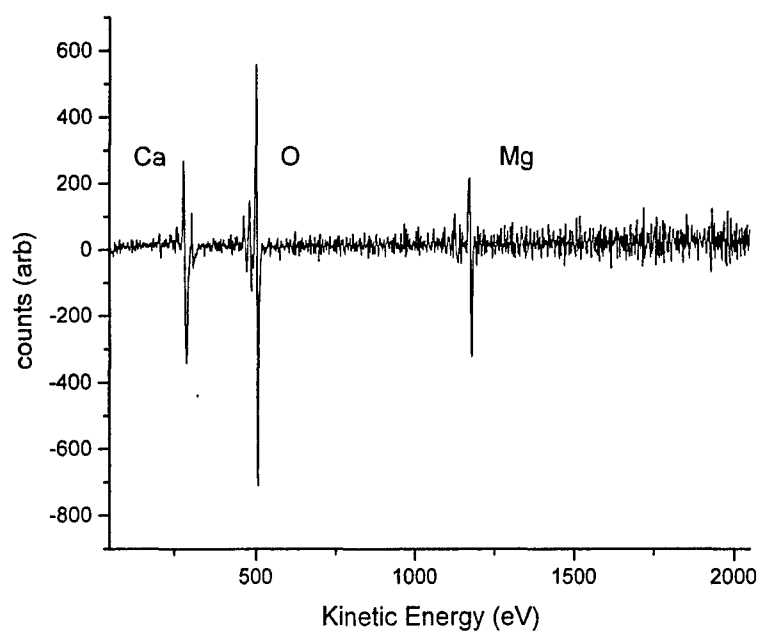


Figure 4.3.24. AES of MgCaO film grown at substrate temperature of 300°C.

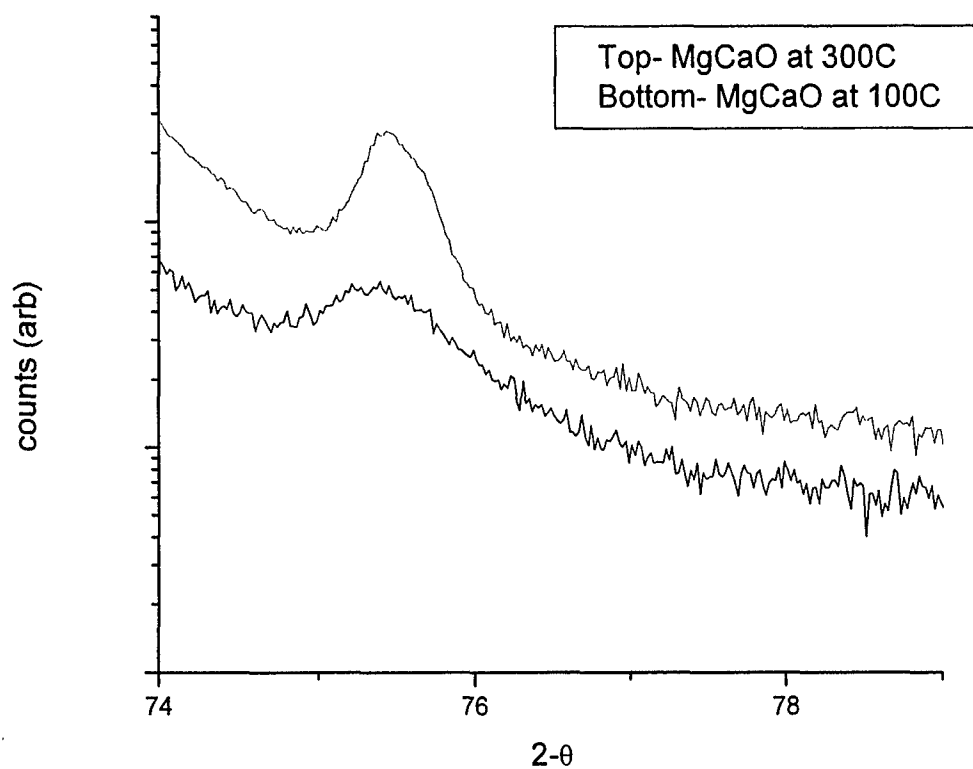


Figure 4.3.25 XRD shows that the peak from the MgCaO film grow at 300°C is much sharper than the MgCaO film grown at 100°C.

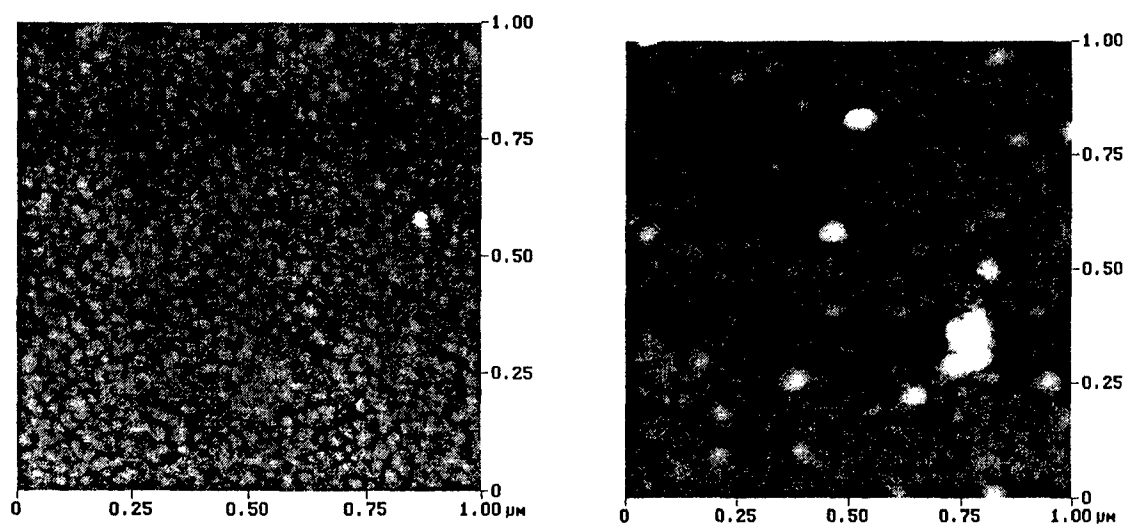


Figure 4.3.26. AFM of MgCaO grown at 100°C, rms = 1.256nm (at left), AFM of MgCaO grown at 300°C, rms = 1.931nm (at right).

In order to reduce the segregation, a digital growth technique was used. Initially conditions were set so that the Mg and Ca fluxes were equal, and the substrate temperature was 300°C. The resulting films were Mg rich, which showed that Ca has a lower sticking coefficient than Mg. Subsequent samples were grown using a progressively higher Ca flux in order to incorporate more Ca into the film and reduce the lattice mismatch. Digital samples were grown at the same fluxes and oxygen pressures as the continuous samples. AFM shows that the digital samples have a slightly smoother surface than the continuous samples. Also the growth rate of the continuous samples is about twice that of the digital samples, which was expected. Due to a combination of the growth rate and the growth sequence, the digital samples all showed a much more uniform depth profile in AES especially near the surface, as shown in Figure 4.3.27. In the continuous samples there is a dip in the oxygen concentration near the surface as well as in the Ca profile. The ratio of oxygen to total metal shows a greater incorporation of oxygen in the digital samples than the continuous samples, as shown in Table IV.

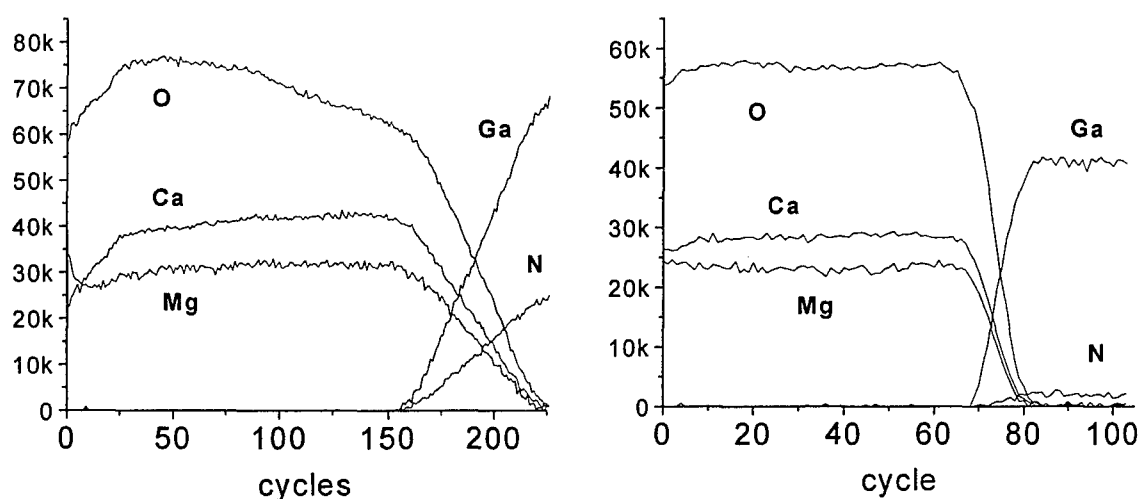


Figure 4.3.27. AES scans of continuously grown sample (at left), and digitally grown sample (at right). Both films were deposited at 300°C under the same conditions.

Table IV. Growth rate, AFM and AES data for MgCaO grown at 300°C.

Growth Method	Mg Beam Equivalent Pressure ($\times 10^{-8}$ Torr)	Ca Beam Equivalent Pressure ($\times 10^{-8}$ Torr)	Growth Rate (nm/min)	RMS roughness (nm)	O/(Mg+Ca) from AES
Continuous	10	9.0	5.6	1.931	0.52
Digital	9.6	8.6	3	0.712	1.40
Continuous	8.0	9.0	5.3	0.774	1.29
Digital	8.0	9.0	1.8	0.554	1.81
MgO ref.	12	---	2.4	1.998	0.50

Powder XRD shows no oxide peaks other than those expected for the MgCaO. The oxide (222) peak is found to shift toward the GaN peak as the amount of Ca incorporated into the film is increased for both the digital and the continuous growth sequences, shown previously in Figure 4.3.22. This peak position is the same for either growth method grown under the same fluxes, Figure 4.3.28. At the highest Ca concentration, the lattice mismatch has been reduced from -6.5% for MgO to -2.05% for the ternary, as shown in Table V. High resolution XRD shows a full width at half maximum (FWHM) of 3542 arcseconds, Figure 4.3.28. Though this is substantially higher than the GaN FWHM of 507 arcseconds, it is a significant improvement over the value of 4327 arcseconds measured for MgO grown on GaN using similar growth conditions.

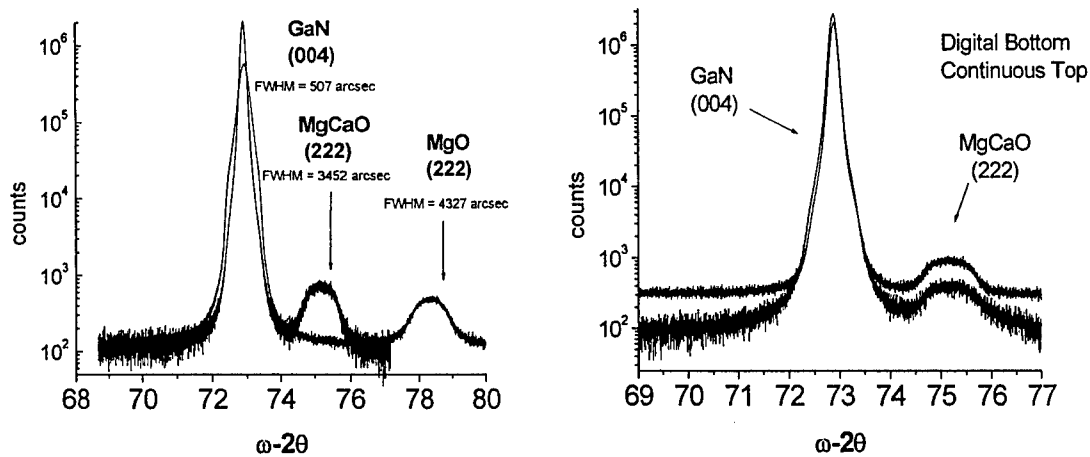


Figure 4.3.28. HR-XRD showing MgCaO and MgO texturing in the (111) direction. Peak positions were the same for the digital and continuous growth techniques under the same growth conditions. The ternary oxide showed a significantly lower FWHM than the binary MgO

Table V. Composition and mismatch for ternary oxides as determined by XRD

layer C- continuous D- digital	2-theta	% Mg	% mismatch to GaN
MgO	78.59	100	-6.45
MgCaO-C	75.43	72.8	-3.11
MgCaO-D	75.41	72.8	-3.09
MgCaO-C	74.79	74.79	-2.40
MgCaO-D	74.47	74.47	-2.05
50/50	~72.9	50	-0.23
CaO	67.375	0	6.86

Similar to the XRD data, XTEM shows improved crystal quality in the ternary as compared to the binary, shown in Figure 4.3.29. In both cases, the oxide /GaN interface is epitaxial. For the binary, continued growth produces a change in microstructure indicative of a nanocrystalline film. For the ternary, this transition is not observed and the overall defect density appears to be significantly lower. This improvement in structural quality is most likely due to the reduction in mismatch for the ternary relative to the binary MgO.

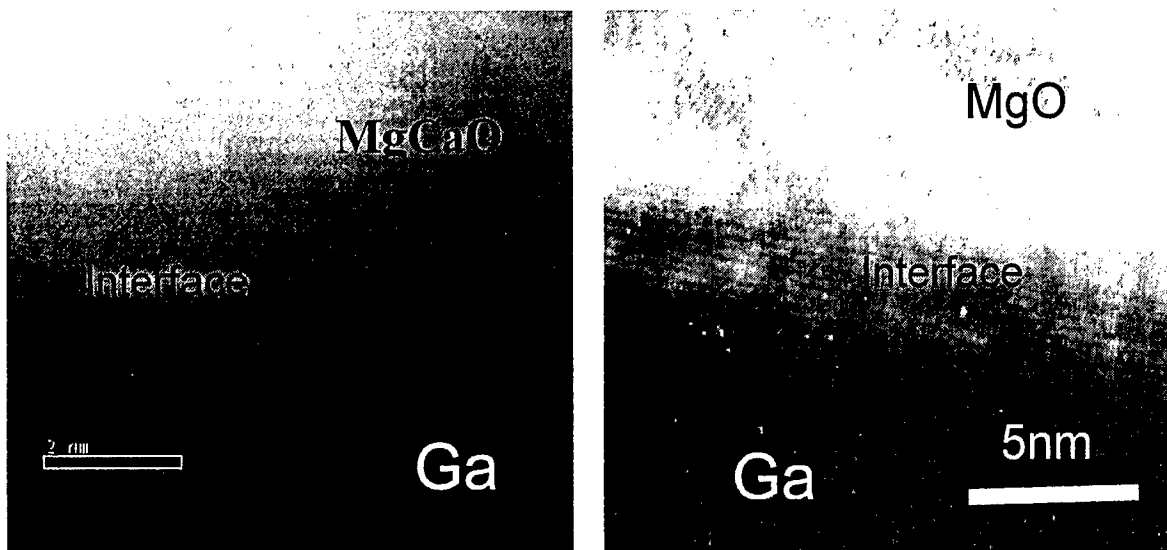


Figure 4.3.29. High resolution XTEM showing the epitaxial nature of the initial oxide layers grown on GaN. The ternary layer, shown at left, shows no evidence of crystallite formation while the MgO layer, shown at right, shows clear evidence of rotational relaxation.

In order to increase the amount of Ca incorporated into the films and reduce the lattice mismatch further, the fluxes of the Mg and Ca were held constant and the length of time the shutters were open was varied. The standard was 10 seconds of Mg followed by 10 seconds of Ca (10/10). This shutter sequence was continued for the entire growth time. The oxygen plasma was kept on the entire growth time. Keeping the cycle time constant at 20 seconds, shutter times of 8 seconds Mg followed by 12 seconds Ca (8/12), and 5 seconds Mg followed by 15 seconds of Ca (5/15) were tried. All samples started with the Mg shutter open first. AFM shows a slight difference in roughness of the surface for the different shutter sequences, Figure 4.3.30. For 10/10 the RMS is 0.790nm, for 8/12 it is 1.081nm, and for 5/15 the RMS is 0.979nm. All of these samples have a 20nm Sc_2O_3 cap. HRTEM shows the oxide to be crystalline and the capping layer to be polycrystalline for the 10/10 shutter sequence.

HRXRD shows the 10/10 sample to have the expected peak position to the right of the GaN (004) peak at 73.9. This corresponds to a composition of 60% Mg and -1.5 % bond mismatch. For the 8/12 shutter sequence more Ca is incorporated and the film is slightly Ca rich. The Mg content goes down to 40.5% Mg and the mismatch is now +0.96%. The 8/12 sample peak shows up as a shoulder on the GaN (004) peak. The 5/15 shutter sequence incorporates even more Ca and has a peak position of 70.175. This

results in a Mg content of 24% and a lattice mismatch of +3.04%. Figure 4.3.31 shows the XRD plots of these 3 samples. Thus it is clear that the mismatch and thus the strain state of the dielectric can be controlled using this approach. The influence of strain on passivation is not currently well understood. Experiments to investigate this issue are in progress.

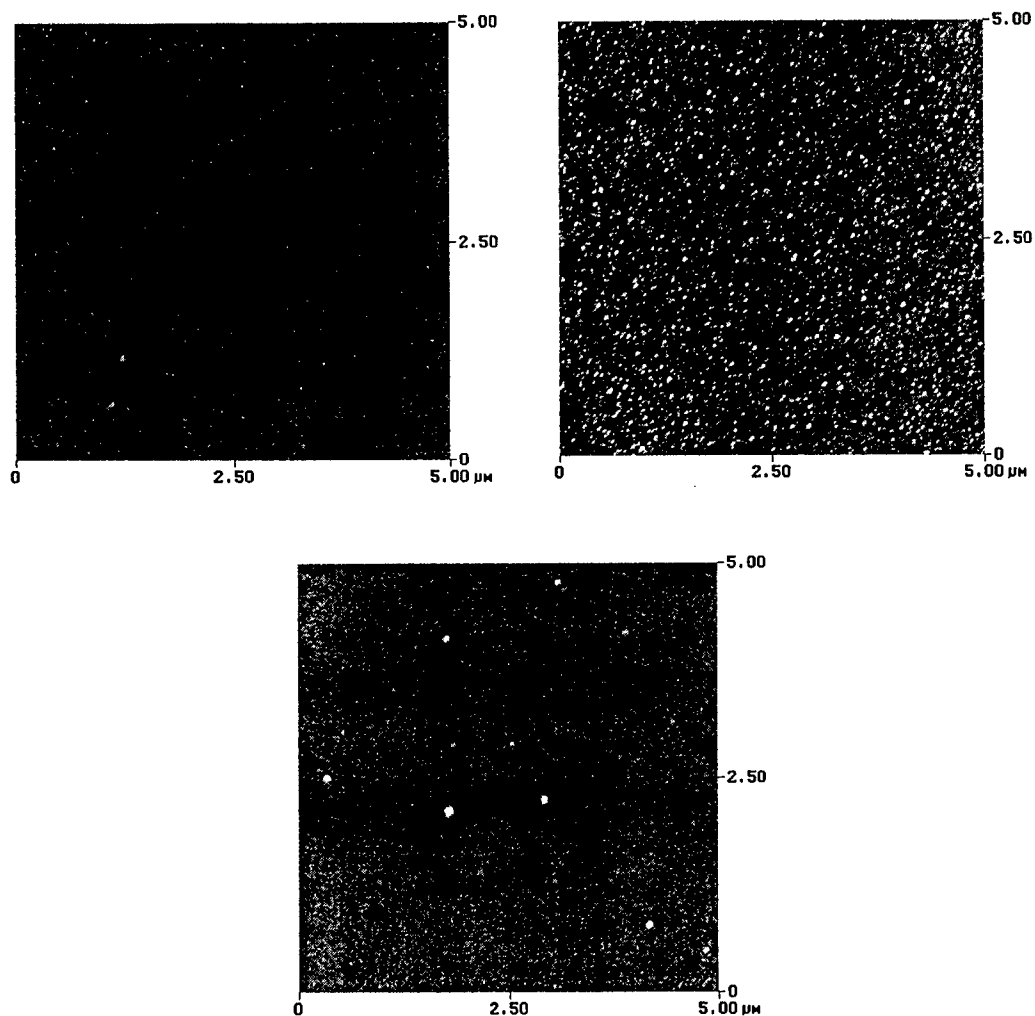


Figure 4.3.30 AFM of capped MgCaO at different shutter sequences. Top left is 10/10 with rms roughness of 0.970nm, top right is 8/12 with rms roughness of 1.081nm, bottom is 5/15 with rms roughness of 0.979nm.

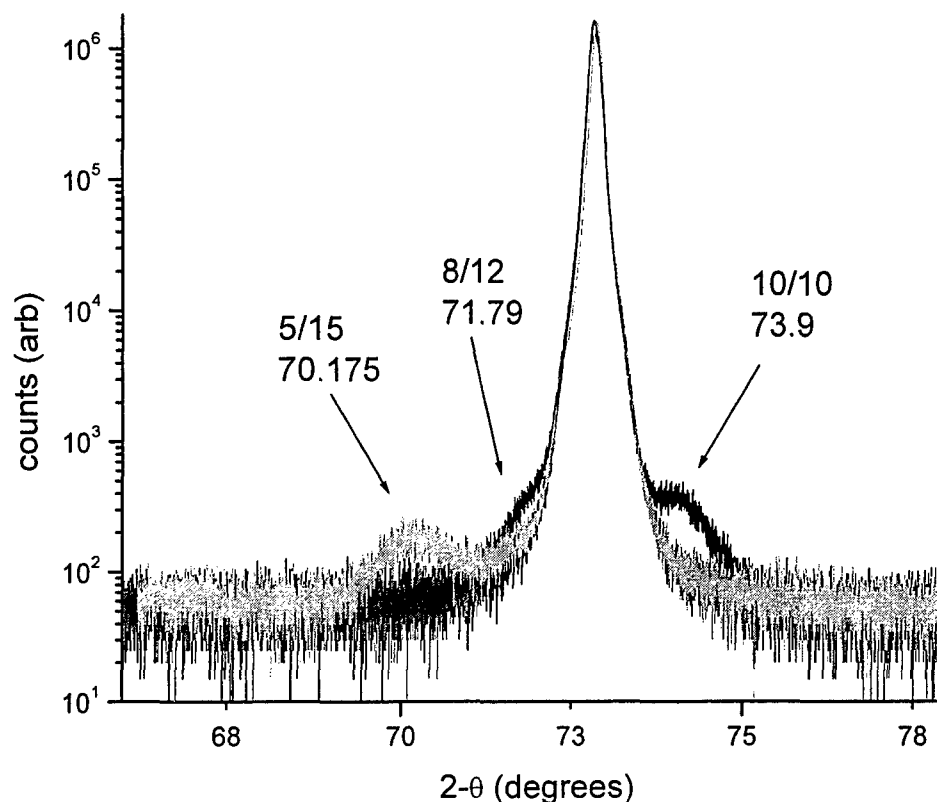


Figure 4.3.31. HR XRD showing change in peak position with change in shutter timing.

4.3.6 UV effects on isolation current

One of the key steps in the passivation process is a UV-ozone treatment on the surface of the processed HEMT wafer. In this process, the processed HEMT wafer is exposed to a high-intensity UV light source that produces ozone in the vicinity of the HEMT wafer. The reason for this treatment is to volatilize any residual carbon from the surface of the wafer. This residual carbon is “left-over” from the photolithography process. We employ this dry technique of carbon removal since a wet technique (acid bath) would damage the metal contact on the surface. One side effect of this process, however, is the emptying of carrier traps in the nitride material. These extra carriers increase the isolation current by over 2 orders of magnitude, Figure 4.3.32. The carrier traps refill in a period of 3 days, with the sample held at room temperature, and the final isolation current returns to the same range as before passivation.

The UV-ozone process was added to other passivation schemes for a comparison. Figure 4.3.33 indicates the UV-ozone cleaning added to passivation with various

dielectrics. It can be seen that the UV-ozone in combination with the crystalline oxides produces the better isolation current, with the reduced lattice mismatched MgCaO providing the lowest isolation leakage. The UV-ozone cleaning greatly improves other dielectric treatments as well. For comparison purposes, SiNx without UV-ozone is also indicated in Figure 4.3.33. Also indicated are more aggressive cleaning recipes with the inclusion of ammonium hydroxide (method 6) or more aggressive oxygen cleaning from an ashing system (method 7). Method 6 showed an improvement over SiNx with no pretreatment, however, the more aggressive ashing treatment increased the isolation leakage. This is most likely due to the ashing treatment creating more dangling bonds on the GaN surface.

The ability to maintain low isolation leakage (nA scale current) has become a standard with the UV-ozone cleaning treatment in combination with the crystalline oxide passivation. This has been reproduced on all HEMT samples that have been passivated with this technique and dielectric, regardless of how the HEMT performed.

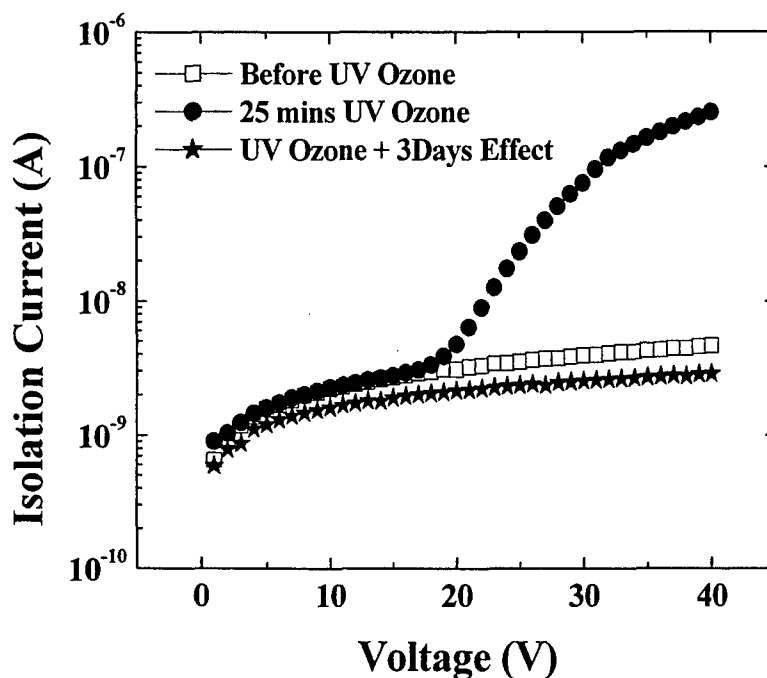


Figure 4.3.32. Mesa isolation current measured before UV exposure, immediately after UV exposure, and 3 days after UV exposure.

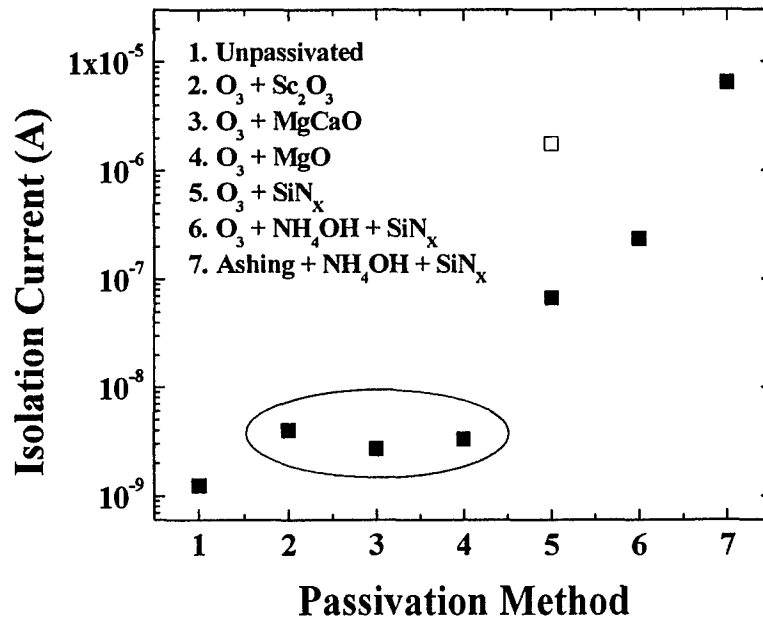


Figure 4.3.33. Isolation current for various dielectrics employing a UV-ozone clean before the dielectric deposition. The open box represents SiN_x without UV-ozone cleaning. ○

4.3.7 Effects of MgCaO composition on passivation and Sc₂O₃ capping

It has been shown that the lattice parameter mismatch has a direct impact on the effectiveness of the passivation dielectric on current collapse mitigation. This was shown by comparison of pulse current vs. dc current of MgO and Sc₂O₃. The MgO has a lattice mismatch of -6.5% and Sc₂O₃ has a 9.1% mismatch with respect to GaN. The smaller mismatch MgO consistently shows a higher passivation effect, by a few percent, over Sc₂O₃. The growth of a reduced lattice mismatch dielectric has been realized by adding calcium to the MgO, forming a ternary MgCaO.

Processed HEMT devices of Al_{0.23}Ga_{0.77}N/GaN structure were passivated with MgO and two different compositions of MgCaO, namely Mg_{0.5}Ca_{0.5}O and Mg_{0.35}Ca_{0.65}O, all at a dielectric thickness of 10nm. The two different calcium concentrations provide for lattice mismatches of approximately -1.0% and +2.0%. These values were measured by growing thicker films of the oxide on a GaN substrate under identical conditions and measuring the x-ray diffraction peaks. An additional sample of 5.0nm MgO capped with 5.0nm of Sc₂O₃, for a total dielectric thickness of 10nm was also grown to compare the effect of the capping layer on the passivation. It has been shown that a 5.0nm capping layer of Sc₂O₃ is sufficient to prevent the underlying MgO or MgCaO from degrading due to high temperature annealing or exposure to high humidity at elevated temperatures. The passivation performance is listed in Table VI.

Table VI. Passivation effects of MgO and MgCaO

	Mg _{0.5} Ca _{0.5} O	MgO	Mg _{0.35} Ca _{0.65} O	MgO/Sc ₂ O ₃
% pulse current before	57.0	60.9	55.3	50.2
% pulse current after	88.4	83.3	89.1	76.2
% gain pulse current	31.4	22.3	33.8	26.0
% lattice mismatch	-1%	-6.5%	2%	-6.5%

The calcium addition to the MgO shows a positive effect in the passivation of surface traps. The MgCaO dielectric provides for a increase of more than 30% pulse current, compared to the MgO dielectric that provided for a 20-25% increase. It is interesting to point out that HEMT devices used for the reduced lattice mismatched dielectric testing actually started with a lower, non-passivated, pulse current than the MgO passivated HEMT. This indicates an even larger effectiveness of the reduced lattice mismatch on mitigating current collapse. The sample that received the MgO capped with Sc₂O₃ showed a similar passivation effect compared to the uncapped MgO. This would indicate that the capping layer does not reduce the effectiveness of the MgO passivation layer.

4.3.8 Other applications of oxide and surface treatment recipes

From many of the tasks performed under this contract, improvements in surface treatments and oxide deposition recipes were developed. These recipes were thought to benefit other areas of research and thus were applied. These other areas included mostly sensor technology developed on the GaN device platform. The same surface states that are responsible for the current collapse phenomena also make the nitride material system attractive as sensors. Gallium Nitride based sensors include gas sensors (hydrogen, methane, ozone, carbon monoxide), liquid sensors (pH level, organic solvents, block copolymers) strain sensors and pressure sensors. These sensors are based upon the polarity and piezoelectric nature of the nitride materials.

Many of these projects benefited from recipes developed under this contract and therefore this contract was acknowledged in those publications and presentations.

4.4 Task 4: Electrical and Environmental Stability

4.4.1 Scandium Oxide capping of crystalline dielectrics

As discussed in the proposal, we have observed degradation of the MgO after long term exposure to air. This degradation is believed to be due to interaction with water vapor in the air to form MgOH species. We have found that capping of the MgO, for example with the gate metal in a MOS diode, effectively suppresses this degradation. Thus one approach to achieving long term environmental stability may simply involve capping of the passivation layer with another dielectric. We have begun preliminary studies of the feasibility of capping the MgO with Sc_2O_3 , which is air stable. For this study, Sc_2O_3 was grown on top of our standard MgO/GaN structure at 100°C . These layers were examined using depth profile AES, shown in Figure 4.4.1. In the as-grown state, there was no indication of oxide intermixing. The samples were then annealed at 800°C for 30 seconds in a RTA with a nitrogen ambient and re-examined. There was no indication of oxide intermixing. This suggests that the Sc_2O_3 capping of MgO should provide for a stable structure that will not only survive in ambient conditions but may also allow the structure to survive any needed subsequent HEMT processing as well.

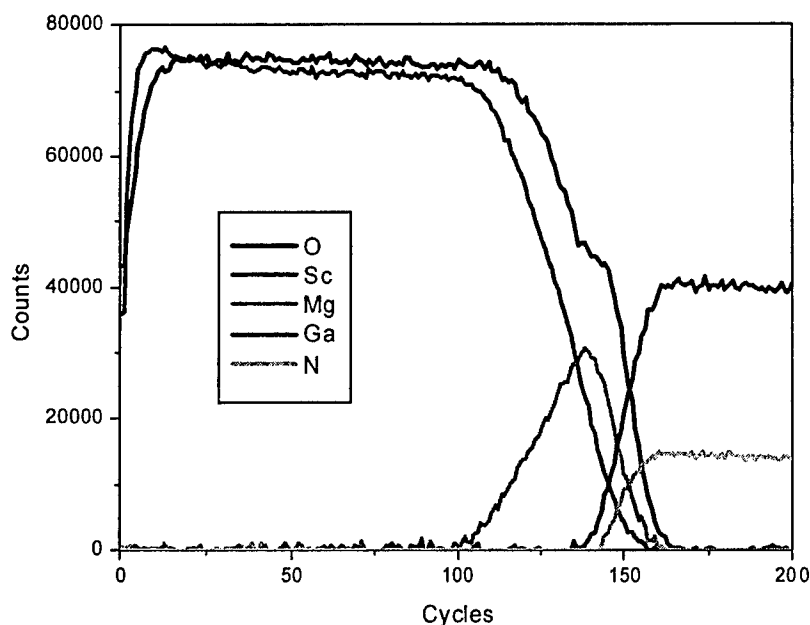


Figure 4.4.1 AES depth profile of $\text{Sc}_2\text{O}_3/\text{MgO}/\text{GaN}$ structure designed to improve environmental stability of MgO passivation layer.

4.4.2 Stability of the crystalline oxides in accelerated aging experiments

Environmental stability is important for the viability of a gate oxide in production and long-term use. If the oxide reacts rapidly upon exposure to light, moisture, or atmospheric gases then it is not viable. The environmental stability of the oxide under study was tested under the accelerated aging conditions of 100% humidity and elevated temperature. A diagram of the accelerated aging experiment is shown in Figure 4.4.2.

The stability of the films was measured as the change of the index of refraction, n , over time. The index of refraction was measured using a J.A. Woollam Spectroscopic Ellipsometer.

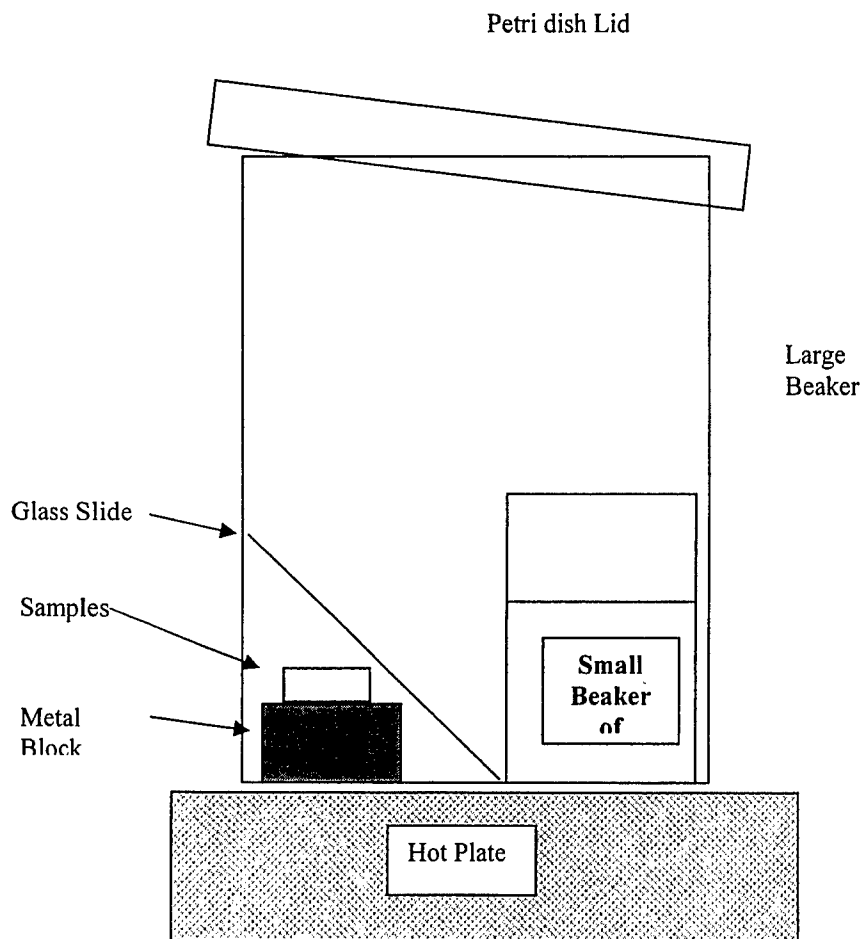


Figure 4.4.2. Accelerated aging experimental set up. The smaller beaker of water inside the larger beaker provides elevated humidity and the hot plate provides elevated temperature. The lid is angled such that condensation will drip down the side opposite of the samples. The glass slide provides protection from random drops of water. The metal block provides heat transfer to the samples while keeping them out of the water that collects on the bottom of the beaker.

Despite the attractive qualities of MgO, it has been found to be environmentally unstable, as shown for example in SEM micrographs of unprotected MgO layers in Figure 4.4.3. The MgO films degrade over time in atmosphere due to the presence of water vapor. The water vapor reacts with the MgO to form magnesium hydroxide, $\text{Mg}(\text{OH})_2$ ^{3,4}. From device processing, it does not appear that the MgO under the metal contacts degrades, only the areas exposed to atmosphere. Capping layers of scandium oxide of various thicknesses have been tried in order to prevent this degradation. Scandium oxide caps of 5nm, 10nm, and 20nm were compared to bare MgO under accelerated aging conditions, Figure 4.4.4. The uncapped MgO shows rapid decrease in

n over time as shown in Figure 4.4.4. A capping layer of 50A greatly improves the environmental stability of the MgO. The 10nm capped MgO shows no apparent degradation over the entire duration of the aging study.

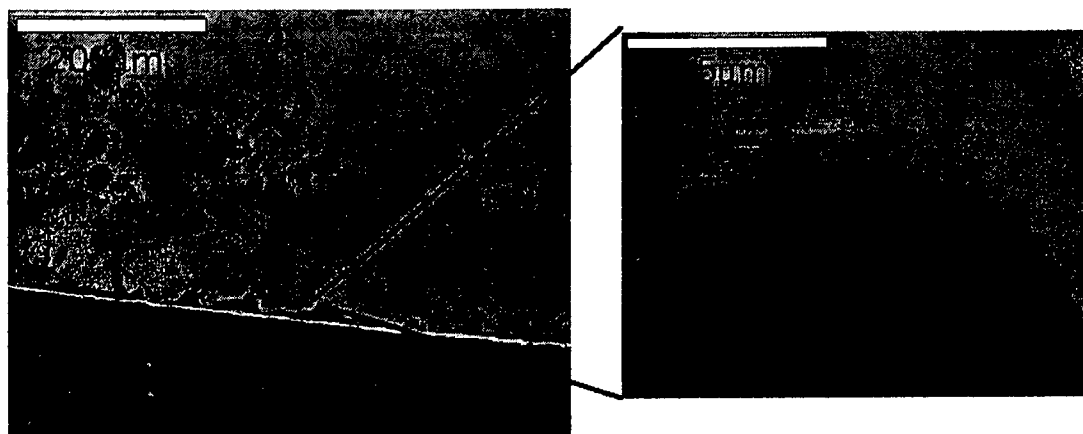


Figure 4.4.3 SEM image of MgO degradation over several weeks at room ambient

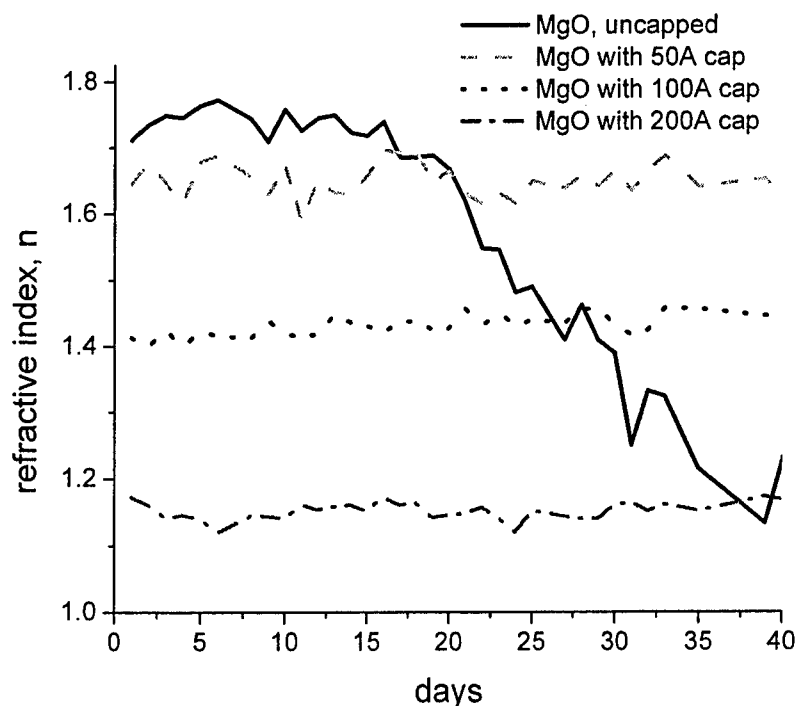


Figure 4.4.4. Ellipsometry of the degradation of MgO with and without a capping layer.

Environmental stability of bare, uncapped MgCaO was compared to MgCaO with a 20nm scandium oxide cap. Uncapped MgCaO degraded more rapidly than the uncapped MgO, Figure 4.4.5. The capping layer of scandium oxide improved the stability of MgCaO. The scandium oxide capping layer was shown to reduce the degradation of the oxides due to atmosphere.

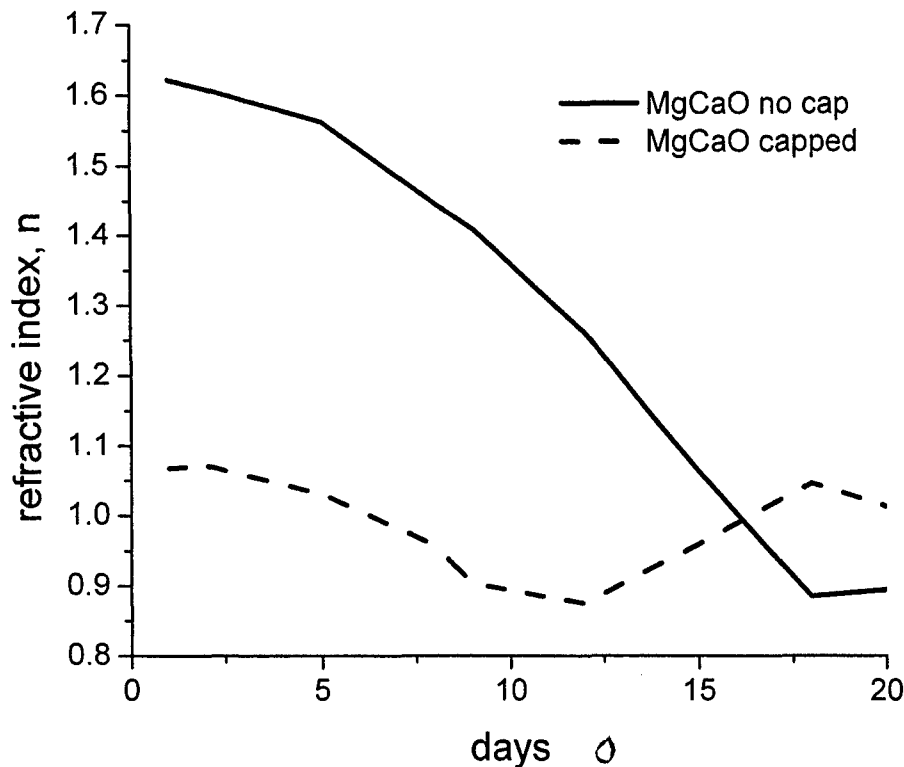


Figure 4.4.5. Ellipsometry of the degradation of MgCaO with and without capping layer.

The thermal stability of the dielectric is important for both operation and processing. If the oxide degrades upon exposure to moderate temperatures over an extended time then the oxide is not suitable due to degradation at operational temperatures. More importantly if the oxide degrades upon annealing at elevated temperatures of up to 1000°C then processing limitations may become an issue, as activation and implant anneals are typically done at elevated temperatures. The oxide films were annealed in an RTA at 1000°C for 2 minutes to test their thermal stability. X-ray reflectivity (XRR), was used to measure the interface roughness before and after annealing to determine the thermal stability of the film.

Uncapped MgO showed severe degradation as determined by significant change in film properties after annealing, Figure 4.4.6. The surface and interface roughnesses increased and the density of the oxide layer changed. This is likely due to recrystallization of the MgO since it is polycrystalline. The capping layer seems to reduce these effects, Figure 4.4.7, but the heterostructure is still not stable under these conditions.

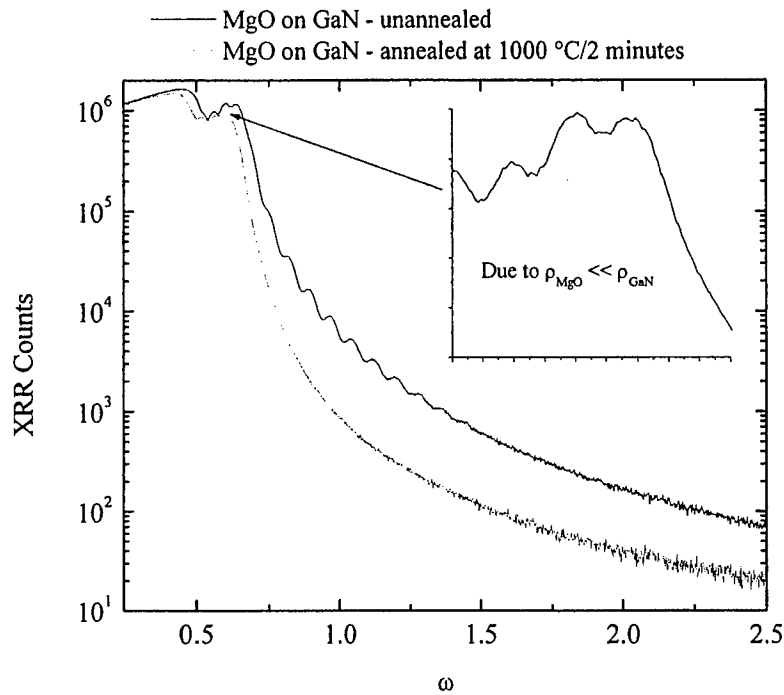


Figure 4.4.6 XRR of MgO uncapped, before and after annealing at 1000°C for 2 minutes.

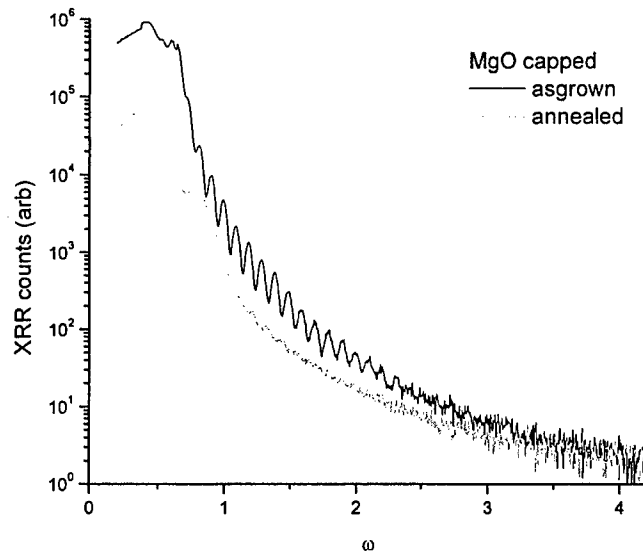


Figure 4.4.7 XRR of capped MgO before and after annealing at 1000°C for 2 minutes.

Uncapped MgCaO also showed degradation after annealing, Figure 4.4.8, but less severely than the MgO. The capped MgCaO shows only slight differences after annealing, Figure 4.4.9. The majority of this difference comes from a change in the capping layer possibly due to recrystallization of the polycrystalline scandium oxide capping layer. The approach of using a reduced defect density single crystal MgCaO

interfacial layer capped with a poly-crystalline Sc_2O_3 layer appears to represent the most stable heterostructure.

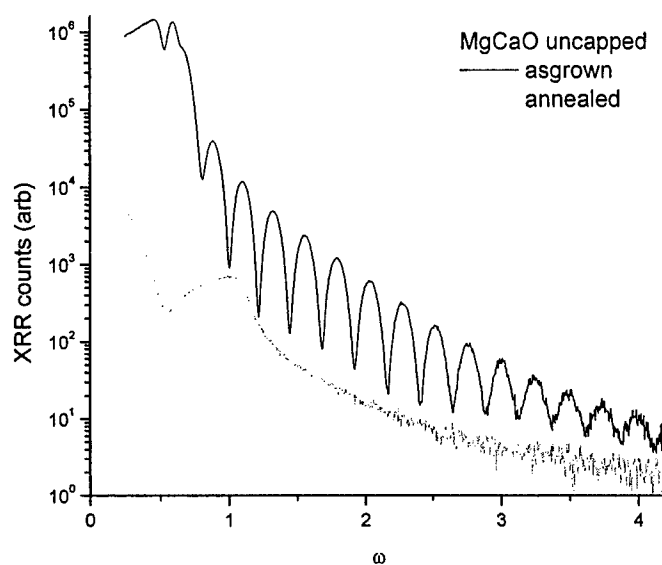


Figure 4.4.8. XRR of MgCaO uncapped before and after annealing at 1000°C at 2 minutes.

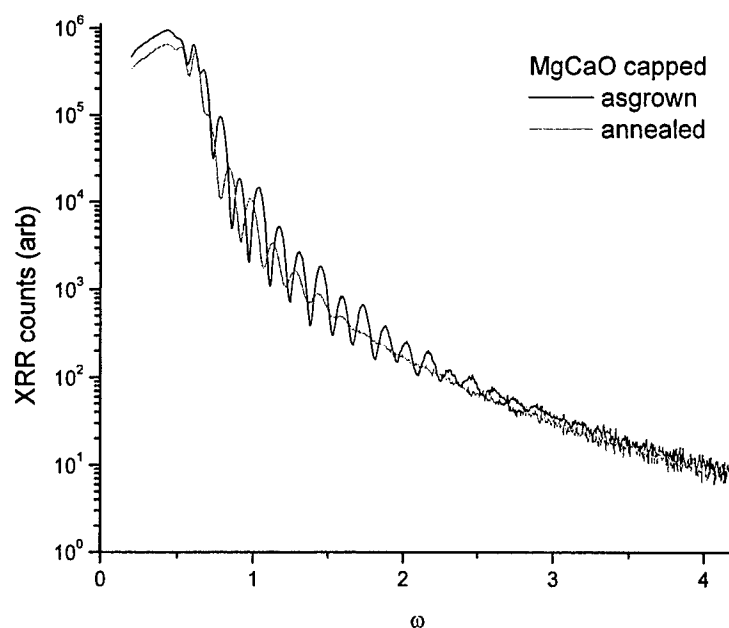


Figure 4.4.9 XRR of MgCaO capped before and after annealing at 1000°C for 2 minutes.

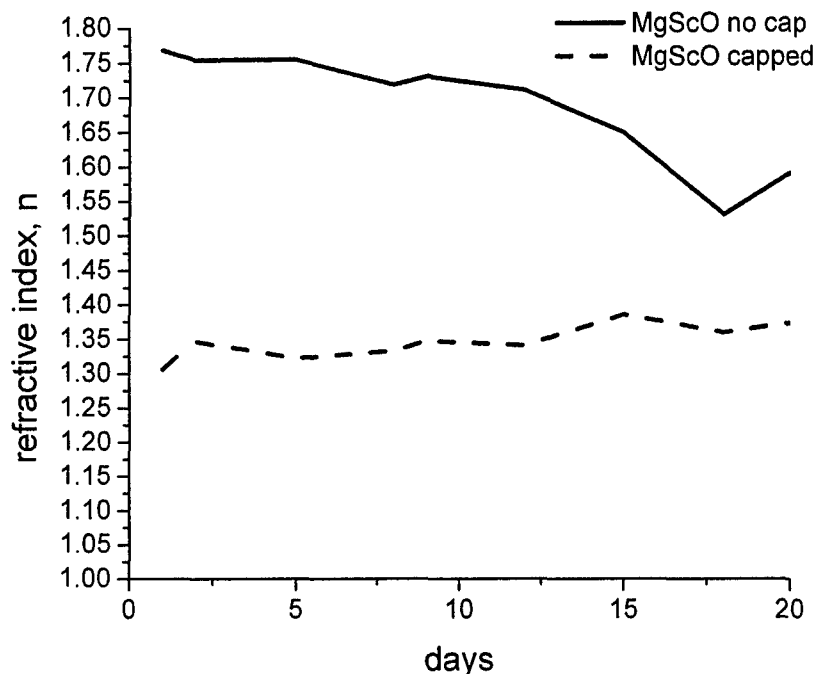


Figure 4.4.4. Ellipsometry of the degradation of MgScO with and without capping layer.

4.4.3 Passivation of Hall effect samples and aging

Hall effect samples were fabricated from unprocessed HEMT material. This material was MOCVD grown on sapphire substrates and consisted of a $2\mu\text{m}$ GaN buffer layer and 24nm $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}$ layer. Conventional van der Pauw patterns with an active area of $4\text{mm} \times 4\text{mm}$ with Ti/Al/Pt/Au corner contacts were used. These samples were tested on a daily basis for a baseline error for the Hall system. The samples were then treated with the standard HEMT cleaning recipe and dielectric deposition recipe as used in the standard passivation: 25 minutes of UV-ozone, 300°C for 5 minutes vacuum anneal, dielectric deposition at 100°C . Samples were then tested for several weeks to determine the effects and stability of the passivation. After this, the samples were placed into an oven at 100°C and 200°C for several more weeks to determine the aging effects on the passivation and HEMT.

The samples were first tested in the Hall effect system to define a baseline for this particular HEMT structure. The sheet carrier density was measured to be $\sim 1.4 \times 10^{13} \text{ cm}^{-2}$. The samples were then subjected to the standard HEMT cleaning process and MgO passivation deposition. An increase in sheet carrier density of $\sim 15\%$ was observed after the passivation process, figure 4.4.10. This increase in sheet carrier density is due to the reduction of surface traps, freeing more carriers in the channel. This trend is consistent with others reported for passivation with SiO_2 and SiNx . These values were stable over several days. One sample was annealed at 100°C in a box furnace under normal ambient

while the other was maintained at room temperature. These samples were tested daily at first, then every few days, for a total of 25 days. No appreciable decrease in the sheet carrier concentration was observed. The aging temperature was then increased to 200°C. The observed sheet carrier concentration indicated a steady decrease of 3% over the 21 day test interval while the control sample showed no indication of deterioration. These results indicate that the passivation is very stable at room temperature and only a slight degradation is observed at 200°C.

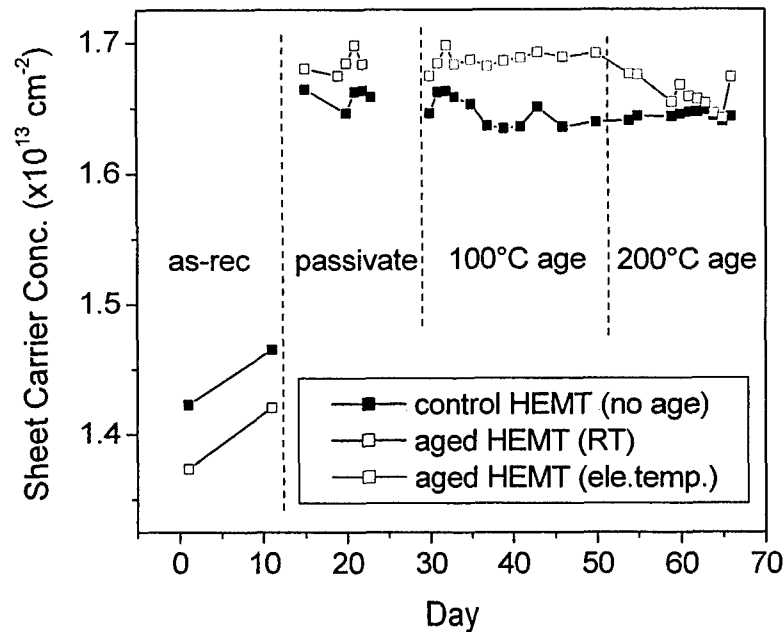


Figure 4.4.10. Hall effect data of a control and aged MgO passivated HEMT.

4.4.4 Passivation of HEMT devices and aging of dielectric films at elevated temperatures

Once the degradation temperature of 200°C was realized, the experiment was replicated on fully processed HEMT devices. The HEMTs were fabricated from MOCVD grown nitride material on sapphire substrates and consisted of a 2µm GaN buffer layer and 24nm Al_{0.23}Ga_{0.77}N layer. These processed devices were diced into sets consisting of two transistors each. One set of devices was without passivation and was used as a control set. Other sets were passivated using various dielectrics, including SiNx and Sc₂O₃ capping layers. These sets of devices were tested to get a base pulse current % (compared to the dc current) and then were aged in a box oven at 200°C.

Figure 4.4.11 shows the non passivated HEMT devices (plot is average of the two transistors) for both the Ids-Vds and figure 4.4.12 shows a SiNx passivated HEMT device

aged under the same conditions. The non-passivated device shows a $\frac{1}{3}$ loss of pulse current after the first week of aging and a $\frac{2}{3}$ loss of pulse current after 4 weeks of aging for a final pulse current of 20% compared to dc current.. The starting as-fabricated pulse current was approximately 60% of the dc current. This SiNx passivated HEMT, with a similar starting pulse current as the non-passivated HEMT, provides an 8% increase in pulse current after passivation. Upon aging, this device set showed a $\frac{1}{4}$ loss of pulsed current after the first week of aging and a $\frac{1}{2}$ loss by week four. The final pulse current was approximately 30% compared to the dc current. This indicates the SiNx passivation provided for some level of protection from the 200°C aging. The SiNx thickness was 10.0nm, similar to the oxide thickness used.

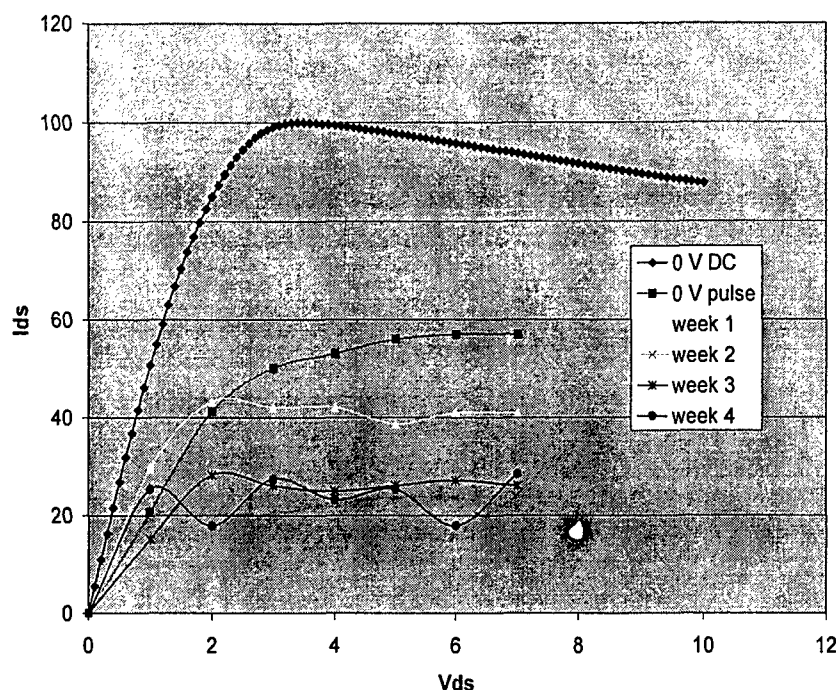


Figure 4.4.11 Elevated aging of non-passivated HEMT device

A third HEMT device set was passivated with a closely lattice matched MgCaO dielectric and, in this case, was capped with Sc_2O_3 for a total dielectric thickness of 10.0nm. The aging data for this device set is presented in figure 4.4.13. Again, for this device, the starting pulse current was 60% compared to the dc current. Therefore all three HEMT sets have the same starting pulse current for ease of comparison. In the case of the lattice matched crystalline oxide, the as passivated device set showed an increase in the pulse current of approximately 10%, similar to the SiNx passivation. However, upon aging, the crystalline oxide passivation actually showed a slight increase in pulse current for week one and a final week four pulse current that is higher than the as-fabricated HEMT devices. There was no visible decrease in pulse current in this devices set as there was in the non-passivated or SiNx device set. Clearly, the advantage of the closely lattice matched crystalline dielectrics is apparent.

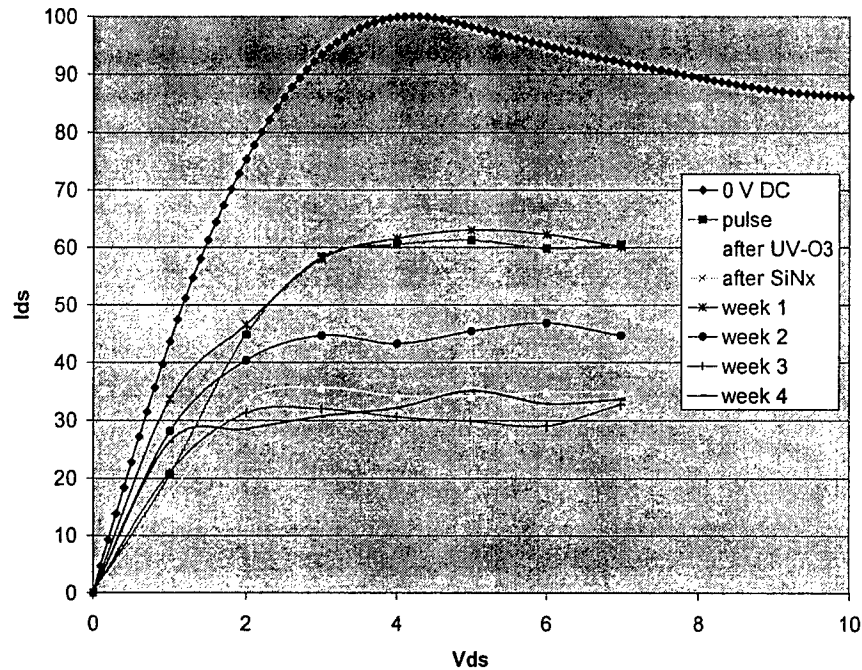


Figure 4.4.12 Elevated aging of SiNx passivated HEMT device

It can be seen in both the SiNx and MgCaO data sets that the pulse current initially decreases after the UV-ozone exposure. This is typically seen in this process and is due to the UV light emptying traps in the GaN buffer that leads to an increase in active buffer traps. These traps typically are refilled in 3 days at room temperature and have been previously reported.

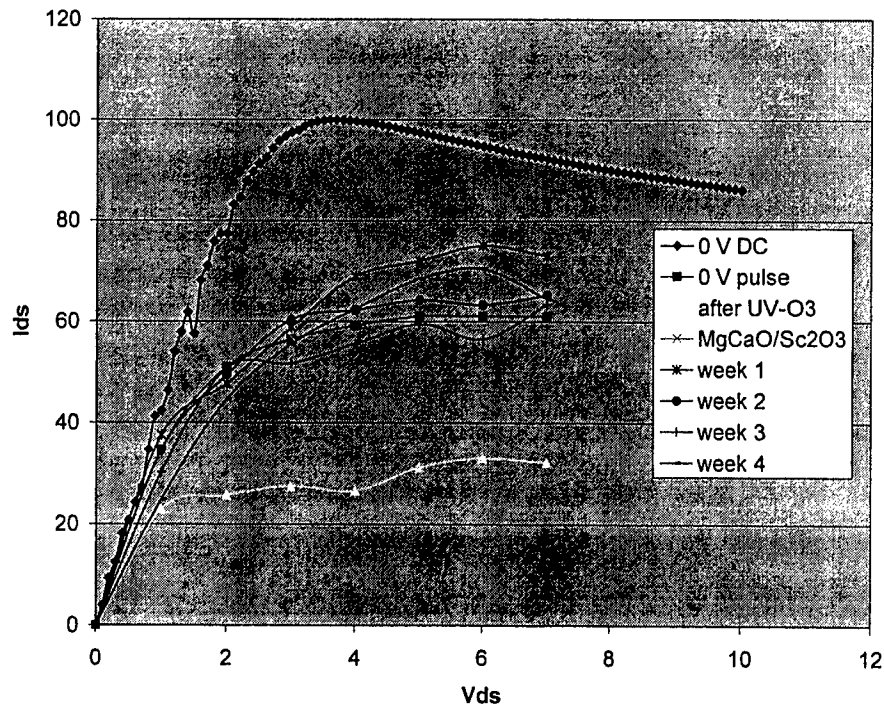


Figure 4.4.13 Elevated aging of MgCaO/Sc₂O₃ passivated HEMT device

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6.0 Publications

1. "Effect of Sc_2O_3 and MgO Passivation Layers on the Output Power of AlGaIn/GaN HEMTs", J. Gillespie, R. Fitch, J. Sewell, R. Dettmer, G. D. Via, A. Crespo, T. Jenkins, B. Luo, R. Mehandru, J. Kim, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy and S. J. Pearton, IEEE Electron Dev. Lett., 23, pp.505-507(2002).
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41. "Improved Oxide Passivation of AlGaN/GaN High Electron Mobility Transistors and Reliability of Passivation"; T. Anderson, B.P. Gila, M. Hlad, A.H. Onstine, A. Gerger, G.T. Thaler, A. Herrero, E. Lambers, C.R. Abernathy, S.J. Pearton, F.

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7.0 Interactions/Transitions

a. Presentations

Meeting: IEEE Biennial Conf. High Performance Devices
Presentation Title: "Comparison of Surface Passivation Films for Reduction of Current Collapse in AlGa_N/Ga_N HEMTs"
Society/Organization: IEEE
Place: Newark, DE
Date: August 2002

Meeting: 2002 MRS Fall Meeting
Presentation Title: "Effects of Plasma Conditions on Structural and Electrical Behavior of MgO Gate Dielectrics Grown by GSMCE on Ga_N"
Society/Organization: Materials Research Society
Place: Boston, MA
Date: December 2002

Meeting: 2002 MRS Fall Meeting
Presentation Title: "Surface Passivation of AlGa_N Terminated and Ga_N Terminated HEMT Structures"
Society/Organization: Materials Research Society
Place: Boston, MA
Date: December 2002

Meeting: 9th Intl. Workshop on Oxide Electronics
Presentation Title: "Growth and Characterization of MgO and Sc₂O₃ Gate Dielectrics on Ga_N"
Society/Organization: none
Place: St. Petersburg, FL
Date: October 2002

Meeting: 203rd Meeting of ECS
Presentation Title: "Progress in Novel Oxides for Gate Dielectrics and Surface Passivation of Ga_N/AlGa_N HFETs"
Society/Organization: The Electrochemical Society
Place: Paris, France
Date: May 2003

Meeting: 2003 MRS Spring Meeting
Presentation Title: "Novel Oxides for Passivating AlGa_N/Ga_N HEMT and Providing Low Surface State Densities at Oxide/Ga_N Interface"
Society/Organization: Materials Research Society
Place: San Francisco, CA
Date: April 2003

Meeting: 204th Meeting of The Electrochemical Society
Presentation Title: "Dramatic Improvements in AlGaN/GaN HEMT Device Isolation Characteristics After UV-Ozone Pre-Treatment"
Society/Organization: The Electrochemical Society
Place: Orlando, Florida
Date: October 2003

Meeting: 204th Meeting of The Electrochemical Society
Presentation Title: "Growth of Magnesium oxide and Scandium Oxide on GaN for use as Gate and Field passivation Dielectrics"
Society/Organization: The Electrochemical Society
Place: Orlando, Florida
Date: October 2003

Meeting: 204th Meeting of The Electrochemical Society
Presentation Title: "GaN Power Rectifiers and Field-Effect Transistors on Free Standing GaN Substrates"
Society/Organization: The Electrochemical Society
Place: Orlando, Florida
Date: October 2003

Meeting: 204th Meeting of The Electrochemical Society
Presentation Title: "Growth of MgCaO on GaN"
Society/Organization: The Electrochemical Society
Place: Orlando, Florida
Date: October 2003

Meeting: 204th Meeting of The Electrochemical Society
Presentation Title: "In-Situ Chemical Surface Treatments for the Removal of AlN/SiC Interfacial Contamination"
Society/Organization: The Electrochemical Society
Place: Orlando, Florida
Date: October 2003

Meeting: 2003 Fall Meeting MRS
Presentation Title: "The Nitride/Oxide Interface: a study for gate dielectrics and field passivations"
Society/Organization: The Materials Research Society
Place: Boston, Massachusetts
Date: December 2003

Meeting: 2003 Fall Meeting MRS
Presentation Title: "Growth of Scandium Magnesium Oxide on GaN"
Society/Organization: The Materials Research Society
Place: Boston, Massachusetts
Date: December 2003

Meeting: 46th TMS Electronic Materials Conference
Presentation Title: "Passivation of GaN and AlGa_N Using Ex-Situ UV-Ozone and MBE Grown Oxides"
Society/Organization: The Minerals, Metals & Materials Society (TMS)
Place: Notre Dame, Indiana
Date: June 2004

Meeting: 2005 Annual Joint Symposium of Florida Chapter of the AVS and Florida Society for Microscopy
Presentation Title: "Novel Oxides for the Passivation of AlGa_N/Ga_N High Electron Mobility Transistor"
Society/Organization: Florida Chapter of the American Vacuum Society
Place: Orlando, Florida
Date: March 2005

Meeting: 2005 Annual Joint Symposium of Florida Chapter of the AVS and Florida Society for Microscopy
Presentation Title: "Laser Drilling For Three-Dimensional Packaging Technology On High Speed RF Communication"
Society/Organization: Florida Chapter of the American Vacuum Society
Place: Orlando, Florida
Date: March 2005

Meeting: 207th Meeting of the Electrochemical Society
Presentation Title: "Novel Oxides and Reliability for the Passivation of AlGa_N/Ga_N High Electron Mobility Transistor"
Society/Organization: The Electrochemical Society
Place: Quebec, Canada
Date: May 2005

Meeting: 47th TMS Electronic Materials Conference
Presentation Title: "Novel Oxide Passivation of AlGa_N/Ga_N High Electron Mobility Transistor And Reliability of Passivation"
Society/Organization: The Minerals, Metals & Materials Society (TMS)
Place: Santa Barbara, California
Date: June 2005

Meeting: 208th Meeting of the Electrochemical Society
Presentation Title: "Improved Oxide Passivation of AlGaIn/GaN High Electron
Mobility Transistors and Reliability of Passivation"
Society/Organization: The Electrochemical Society
Place: LA, California
Date: October 2005

Meeting: 208th Meeting of the Electrochemical Society
Presentation Title: "Thermal Simulations of 3-D Integrated Multi-Chip Module with
GaN Power Amplifier and Si Modulator"
Society/Organization: The Electrochemical Society
Place: LA, California
Date: October 2005

b. Consultative functions

We have been actively collaborating with Bob Fitch and colleagues at WPAFB. This collaboration has included shipment of wafers back and forth between WPAFB and UF and frequent phone calls.

8.0 New Discoveries, Inventions or Patent Disclosures
None

9.0 Honors/Awards
None